Figure 2.1 Magnetic RAM construction.
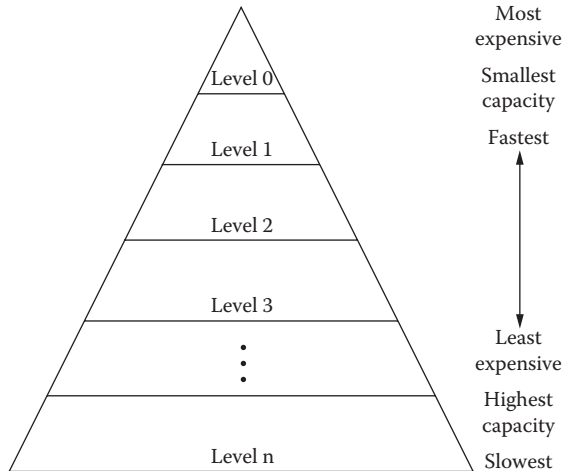
002x001.eps

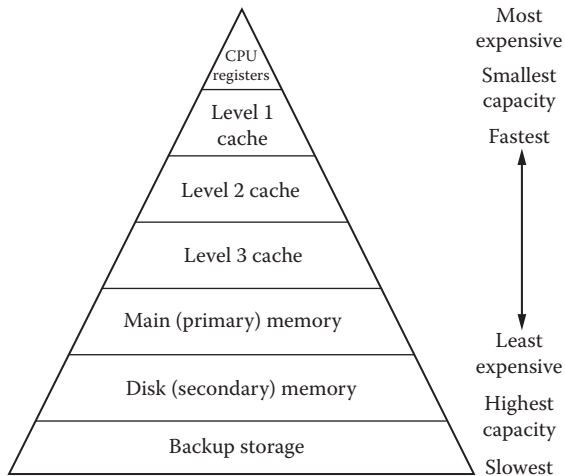Figure 2.2 Memory hierarchy (conceptual).

002x002.eps

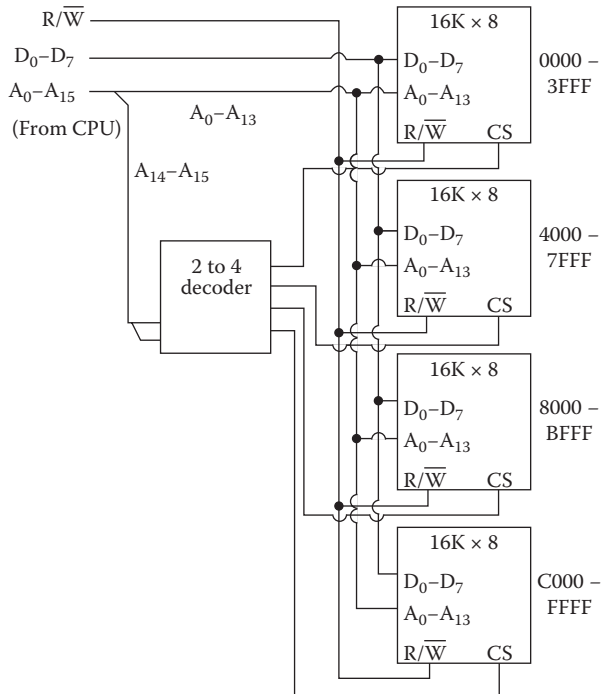Figure 2.3 Memory hierarchy (typical of modern computer systems).

Figure 2.4 Simple memory system using high-order interleaving.

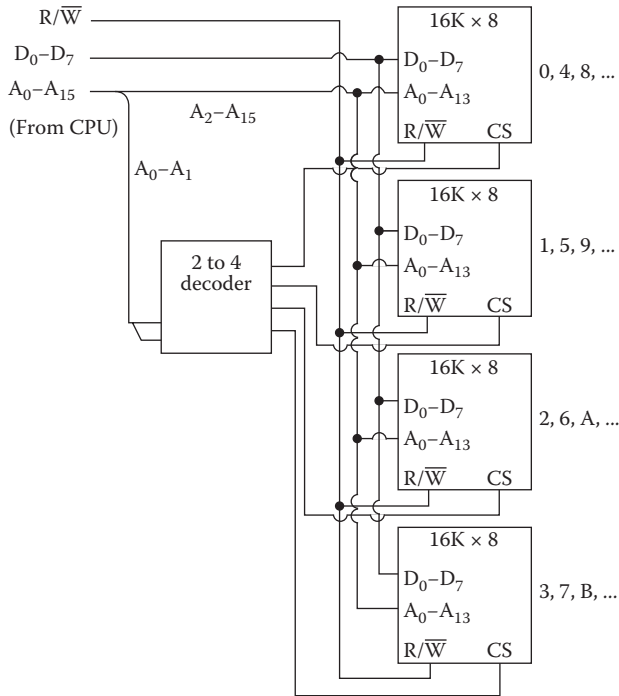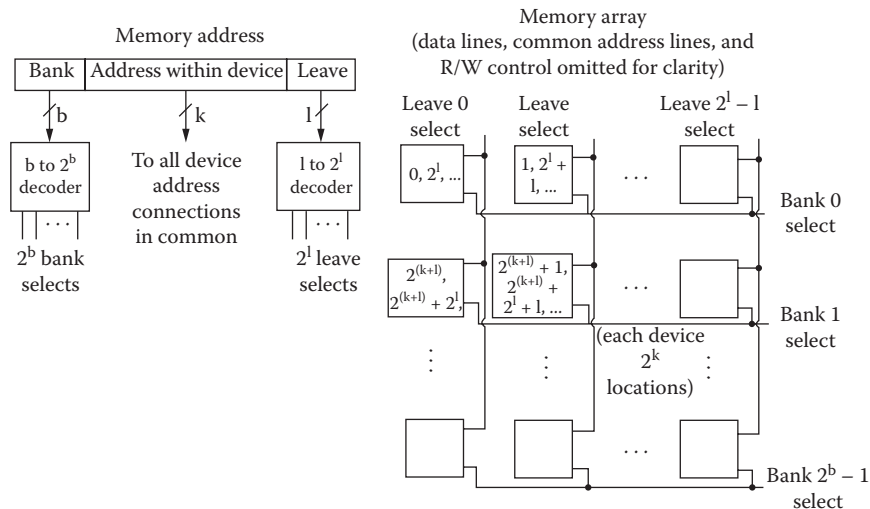Figure 2.5 Simple memory system using low-order interleaving.

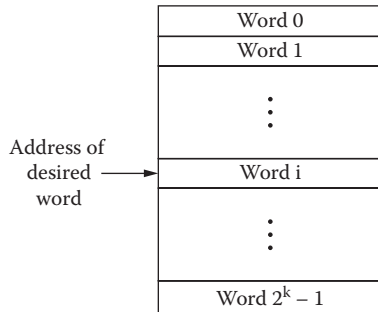Figure 2.6 Memory system using both high- and low-order interleaving.

Word 0
Word 1
$\vdots$
Word i
$\vdots$
Word $2^k - 1$

Address of desired word →

Figure 2.7 Memory access by word slice.

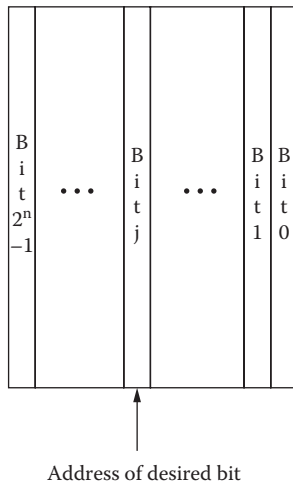002x007.eps

Address of desired bit

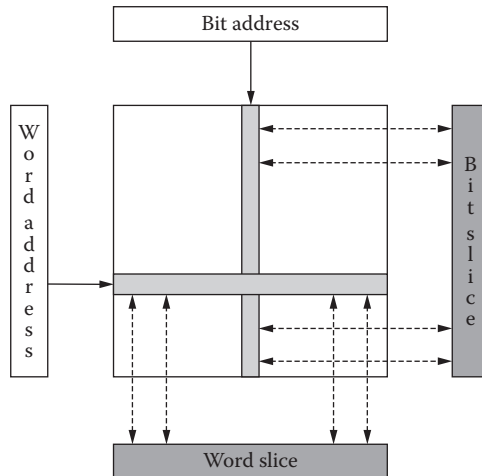Figure 2.8 Memory access by bit slice.
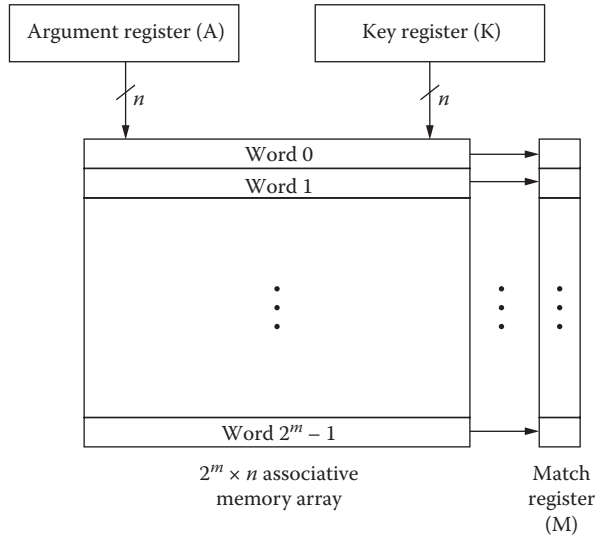
Figure 2.9 Orthogonal memory.

002x009.eps

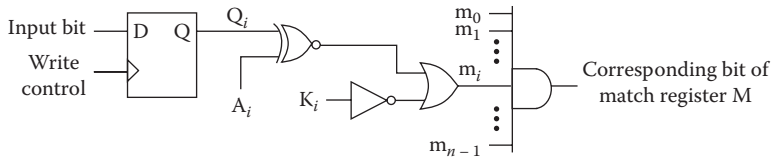Figure 2.10 Associative memory block diagram.

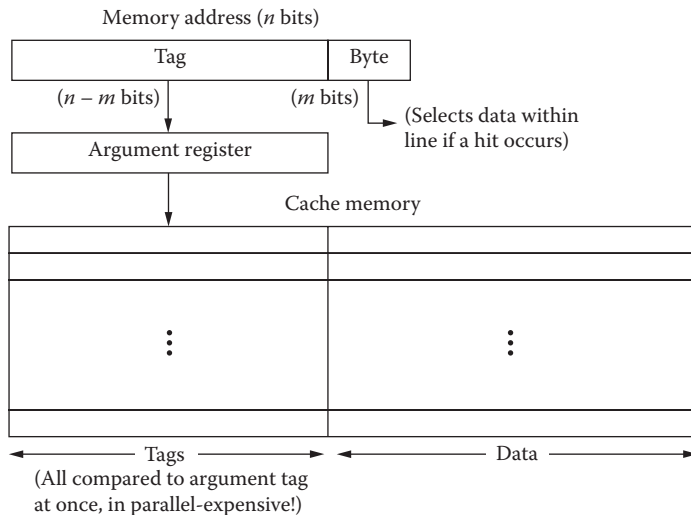Figure 2.11 Associative memory cell logic.

002x011.eps

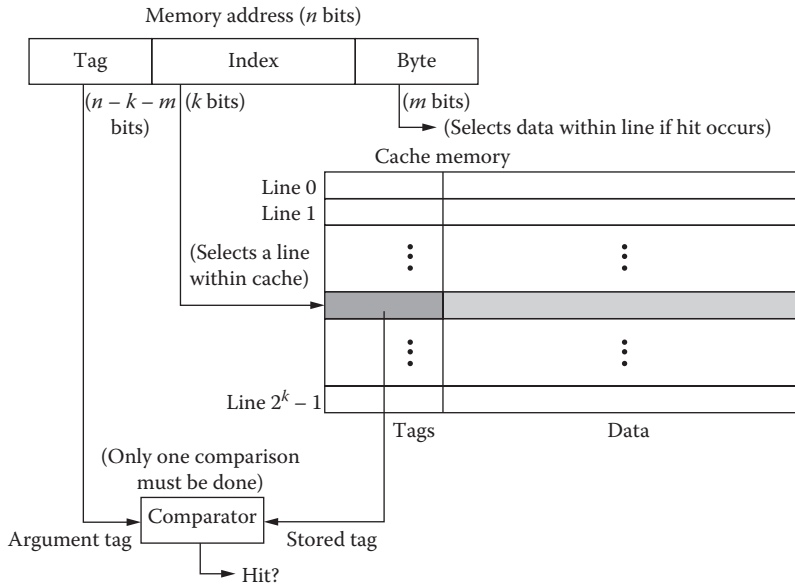Figure 2.12 Fully associative cache.

Figure 2.13 Direct-mapped cache.
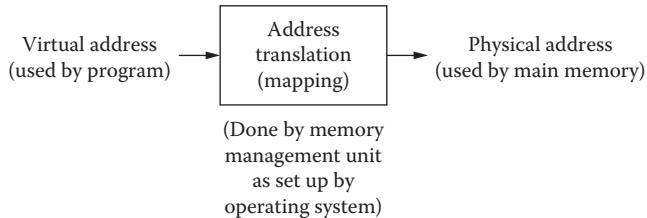
Figure 2.14 Two-way set-associative cache.

Figure 2.15 Address translation in a system with virtual memory.

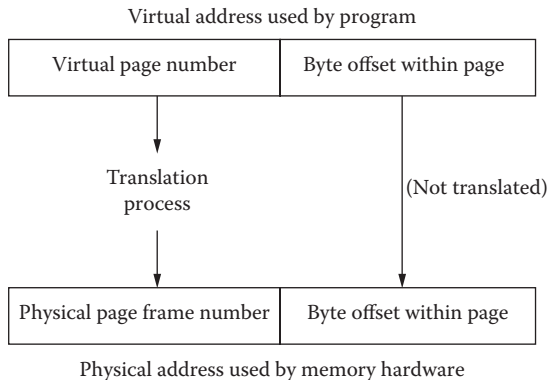002x015.eps

Virtual address used by program

Virtual page number	Byte offset within page

Translation
process

(Not translated)

Physical page frame number	Byte offset within page

Physical address used by memory hardware

Figure 2.16 Address translation in a system with demand-paged virtual memory.

002x016.eps

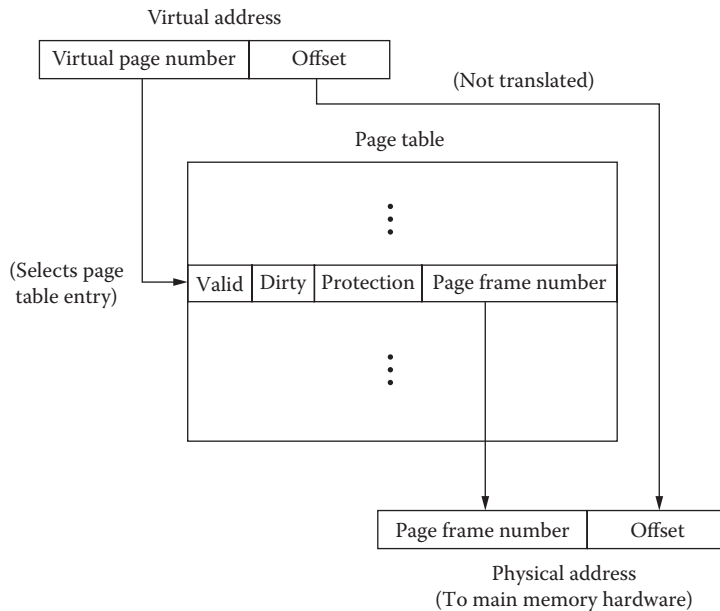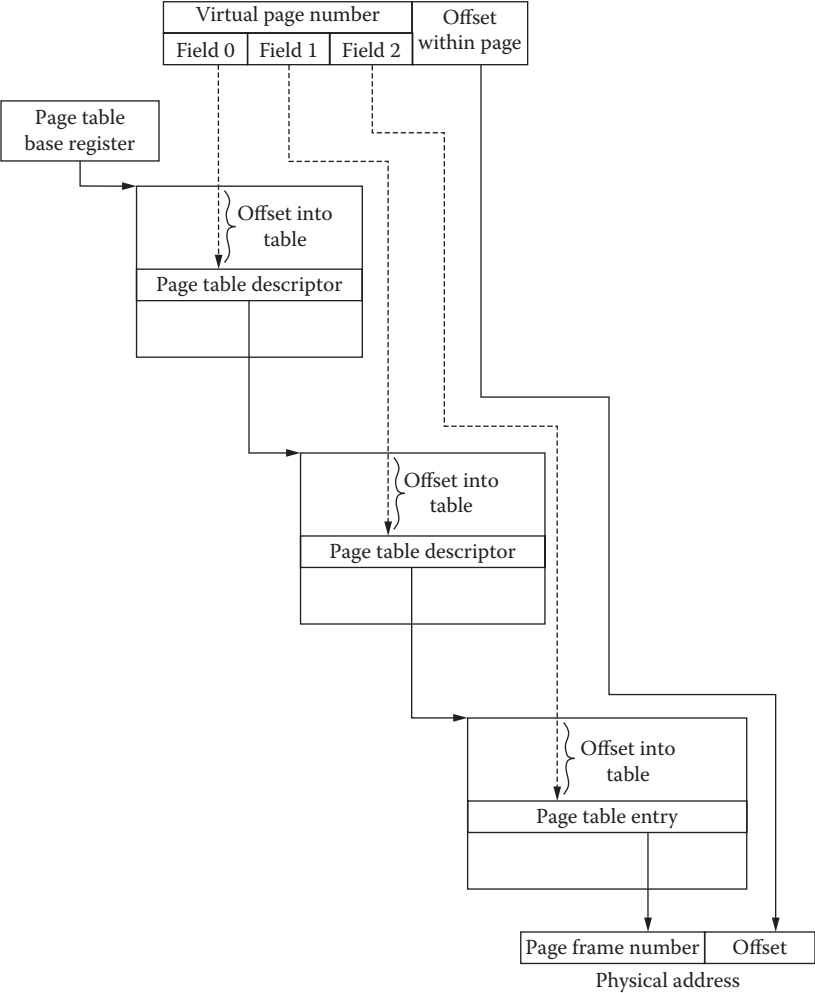Figure 2.17 Table lookup for address translation in a paged system.

Figure 2.18 Multiple-level table lookup in paged system.

Logical address used by program

Logical segment number	Byte offset within segment

Translation
process

Segment starting address
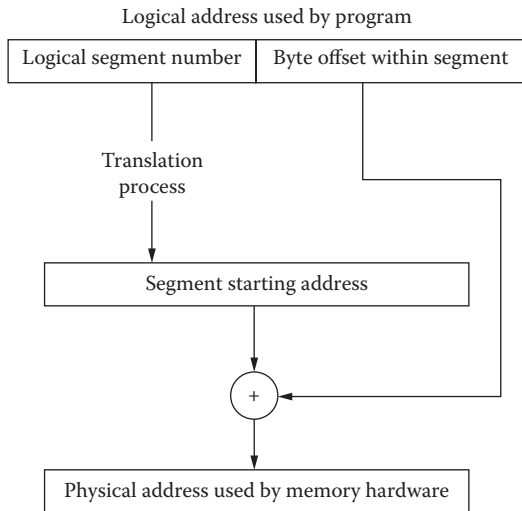
+

Physical address used by memory hardware

Figure 2.19 Address translation in a system with demand-segmented virtual memory.
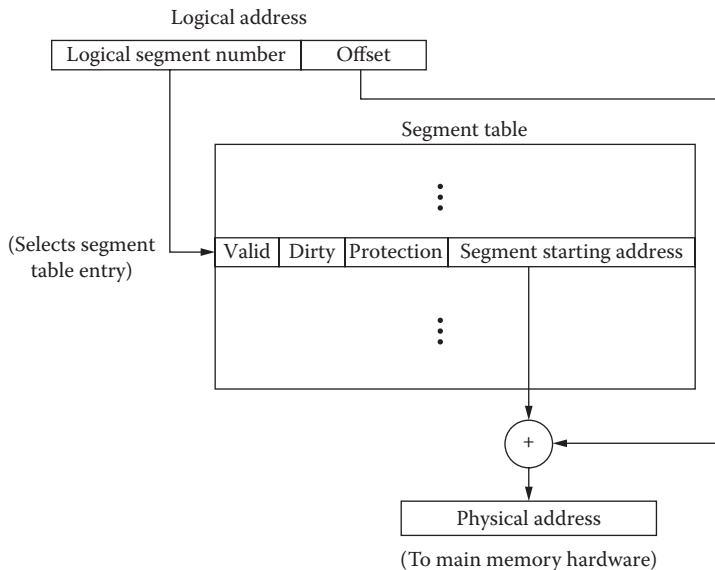
002x019.eps

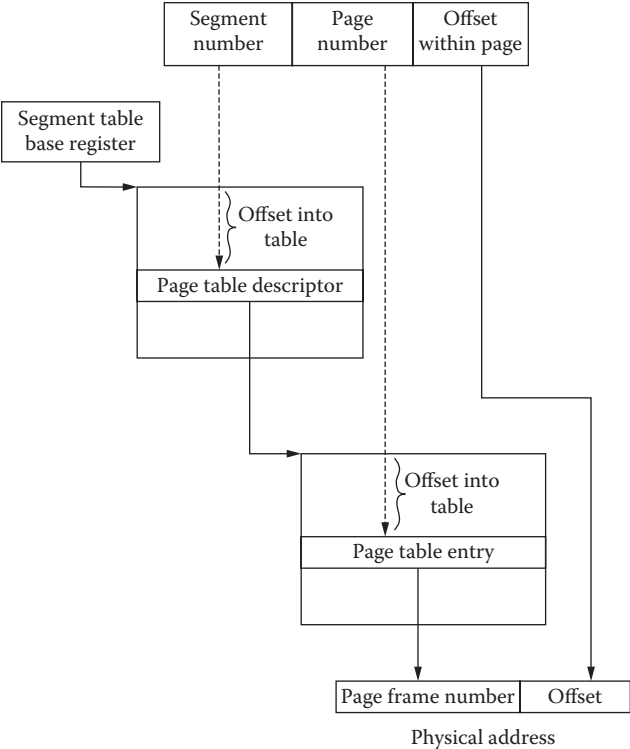Figure 2.20 Table lookup for address translation in a segmented system.

Figure 2.21 Address translation in a system using segmentation with paging.