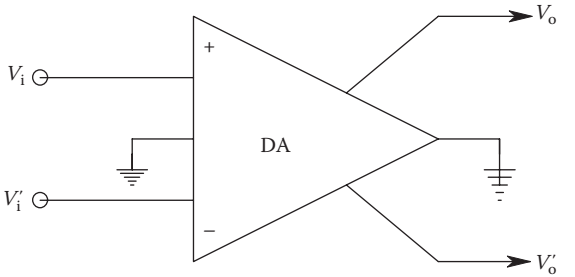


Figure 2.1
Symbol for a generalized DA: note that it is a four-port circuit (V_i, V_i', V_o, and V_o').

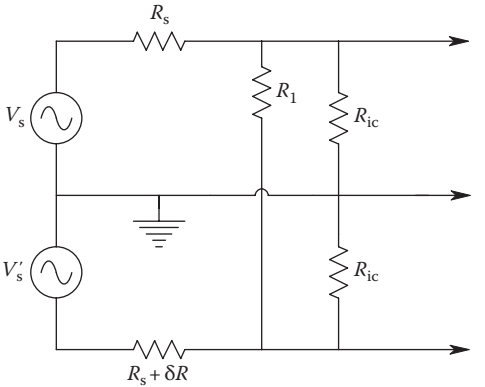


Figure 2.2
DA input circuit at DC, showing source resistance unbalance.

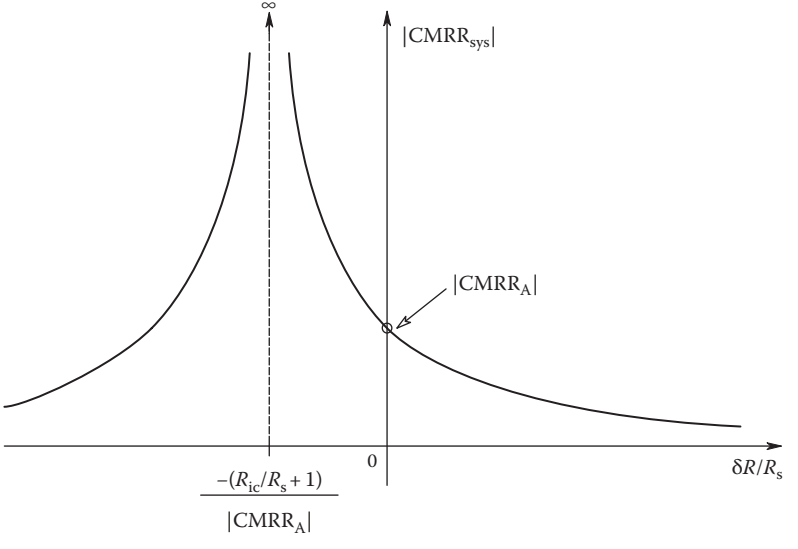


Figure 2.3
DA CMRR magnitude vs. fractional unbalance in source resistance, $\Delta R_s/R_s$.

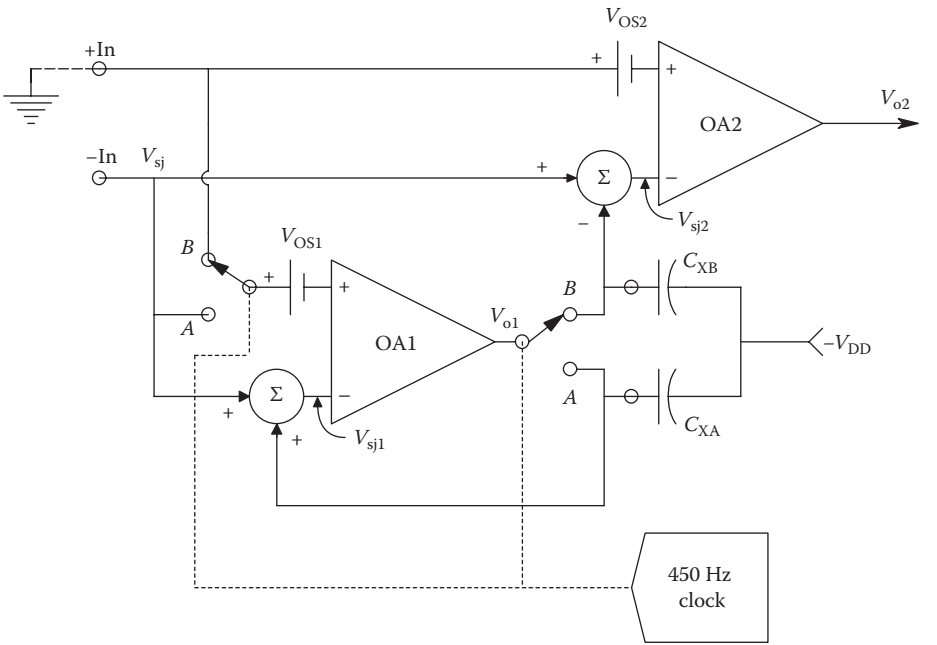
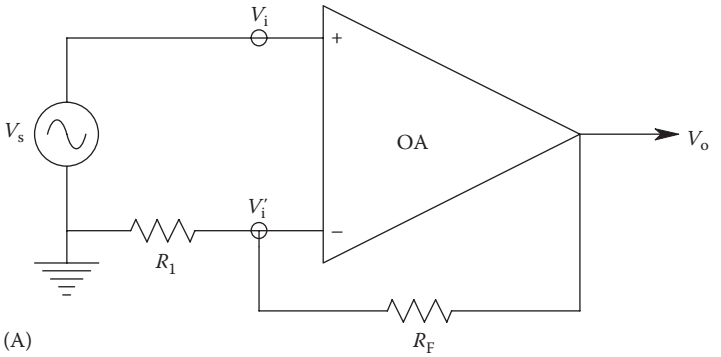


Figure 2.4
Simplified circuit of a Texas Instruments' TLC2652 CSOA.



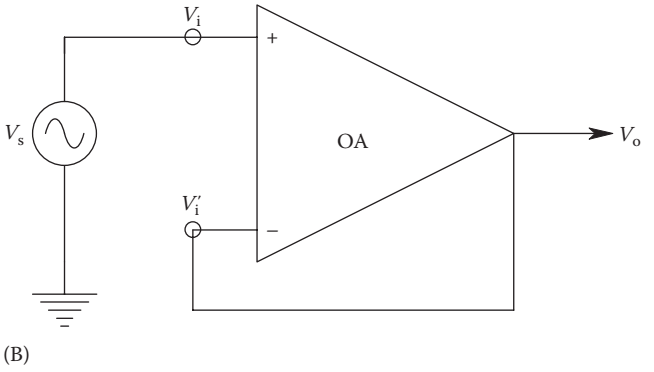


Figure 2.5
(A) A noninverting OA circuit with gain set by R_1 and R_F. (B) Unity-gain buffer OA circuit.

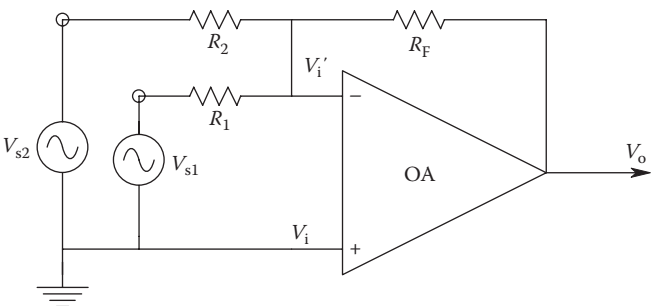


Figure 2.6
Inverting, summing OA configuration.

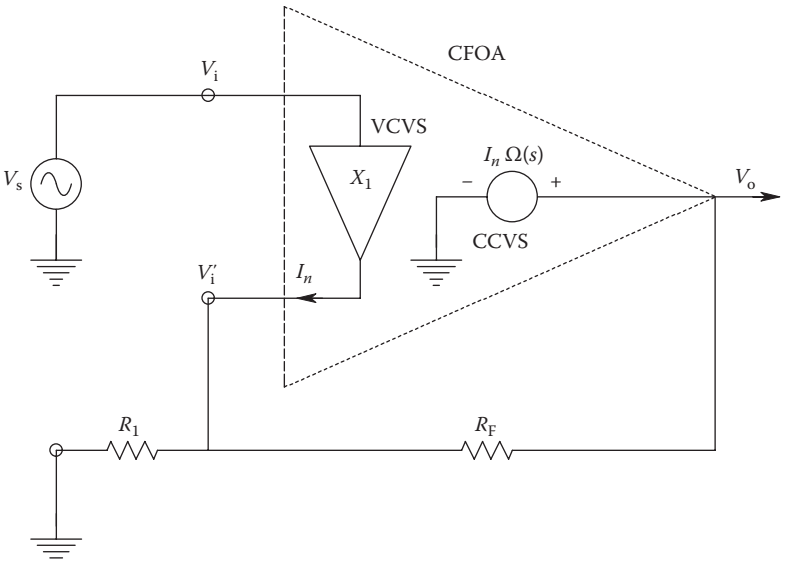


Figure 2.7
A noninverting amplifier circuit using a CFOA.

002x007.eps

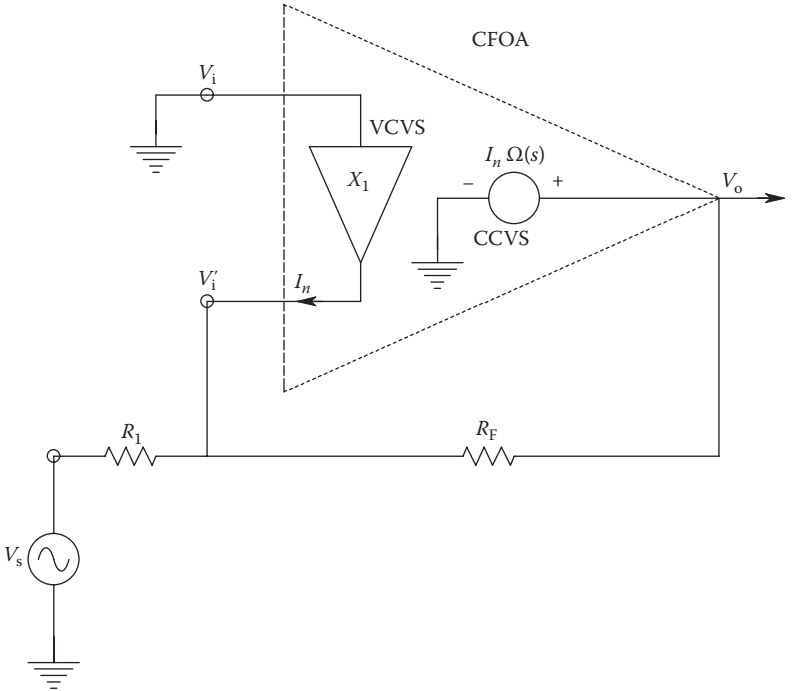


Figure 2.8
An inverting amplifier circuit using a CFOA.

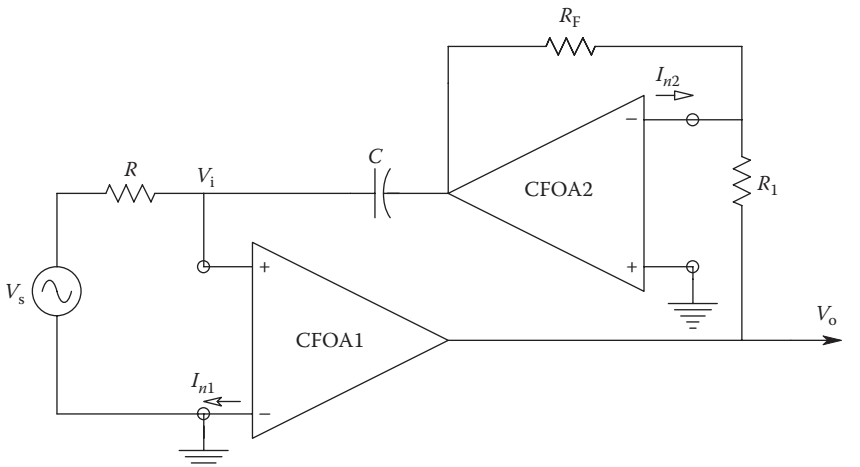


Figure 2.9
A noninverting integrator using two CFOAs.

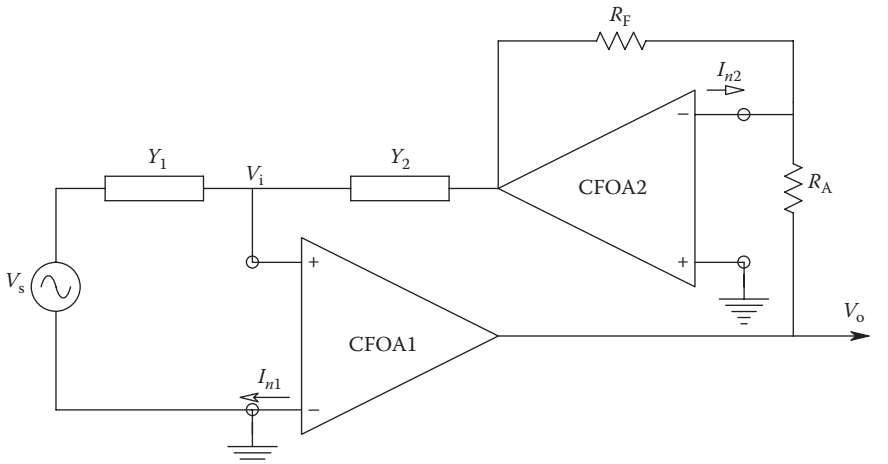


Figure 2.10
A general, noninverting feedback amplifier circuit using two CFOAs.

002x010.eps

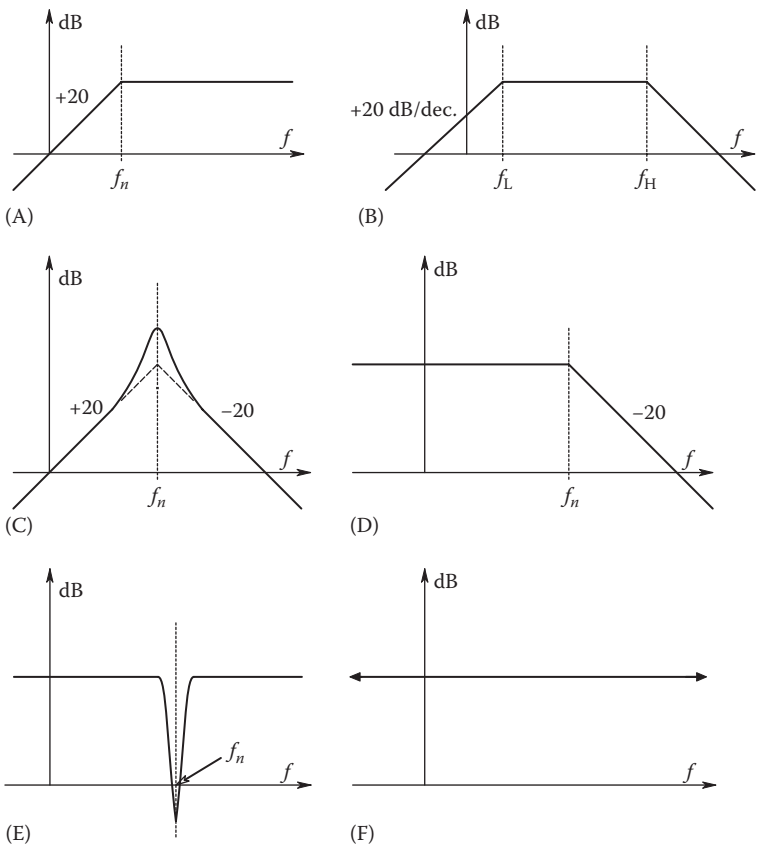


Figure 2.11
Bode asymptotes of common types of filters: (A) HPF. (B) Broad BP. (C) Narrow (tuned) BP. (D) LPF. (E) Band-reject or notch. (F) All-pass (flat amplitude passband, phase is frequency dependent).

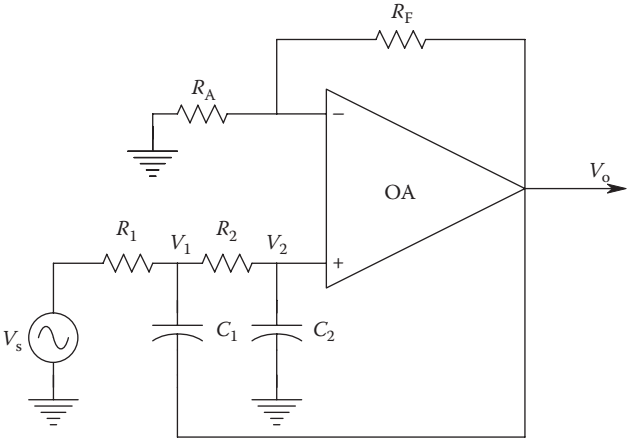


Figure 2.12
A Sallen and Key quadratic LPF.

002x012.eps

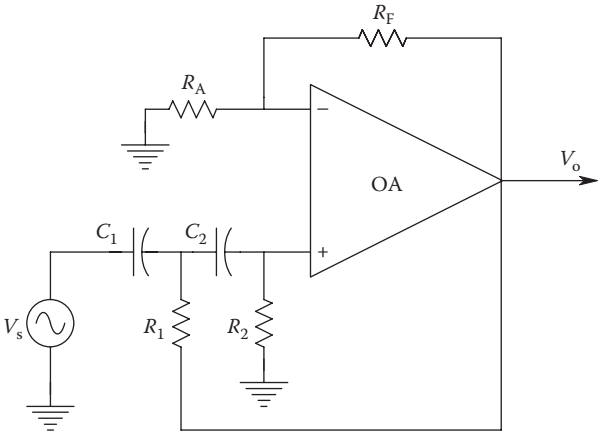


Figure 2.13
A Sallen and Key quadratic HPF.

002x013.eps

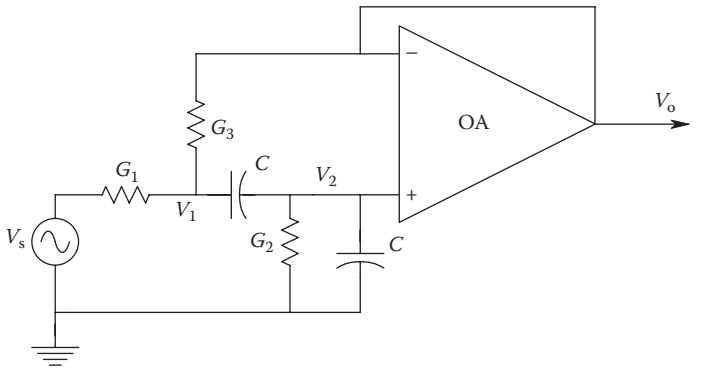


Figure 2.14
A controlled-source, quadratic BPF.

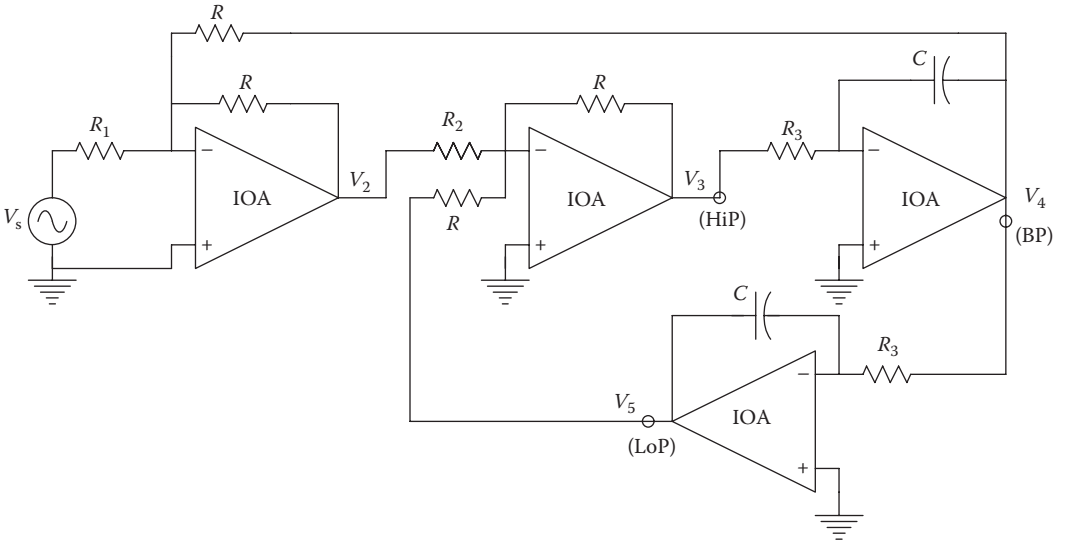


Figure 2.15
A two-loop, biquad AF.

002x015.eps

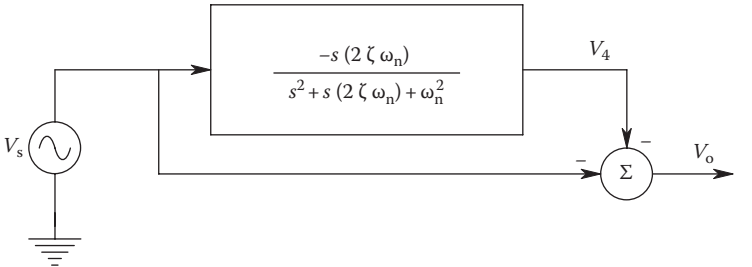


Figure 2.16
Block diagram for a biquad notch filter. V_4 is the inverting BP output of the two-loop biquad filter of Figure 2.15.

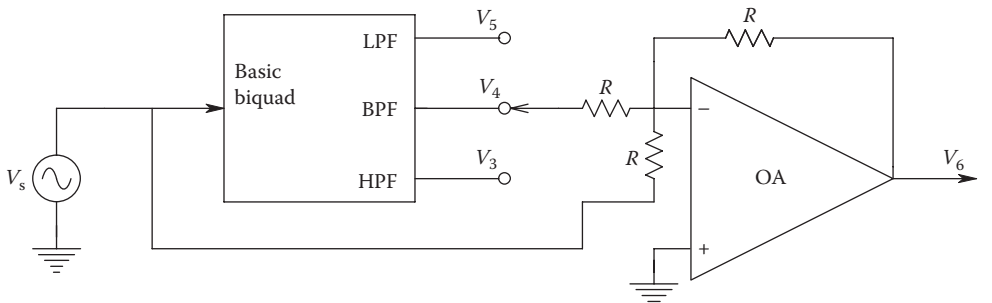


Figure 2.17
Realization of a biquad notch filter using the basic two-loop biquad of Figure 2.15.

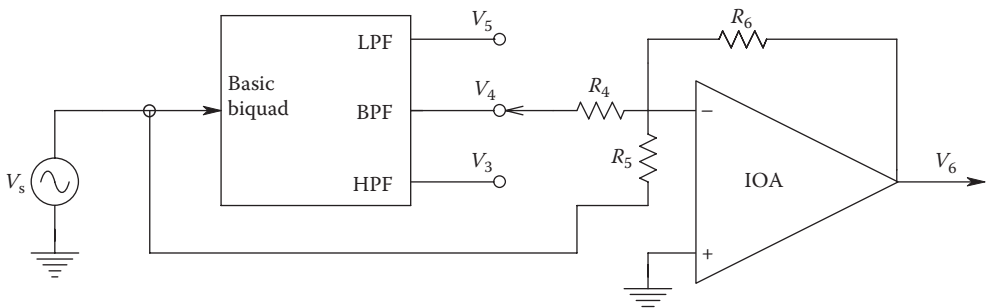


Figure 2.18
Realization of a biquad all-pass filter. See text for special relations for R_4, R_5, and R_6.

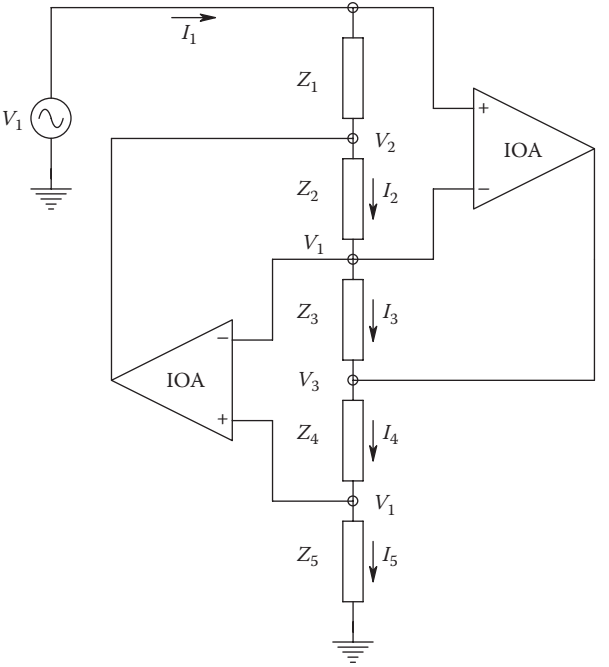


Figure 2.19
The basic GIC circuit architecture.

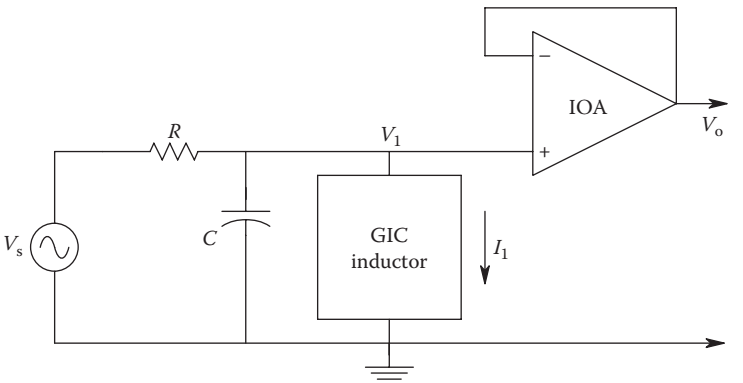


Figure 2.20
A tuned, quadratic BPF using a GIC as a (synthesized) low-loss inductor.

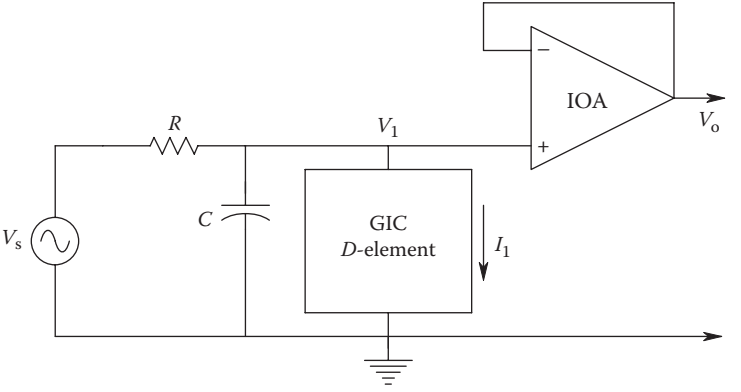


Figure 2.21
A quadratic LPF realized with a GIC FDNR element.

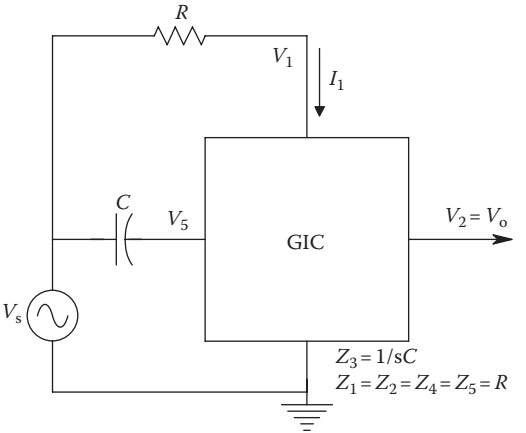


Figure 2.22
A GIC-derived all-pass filter.

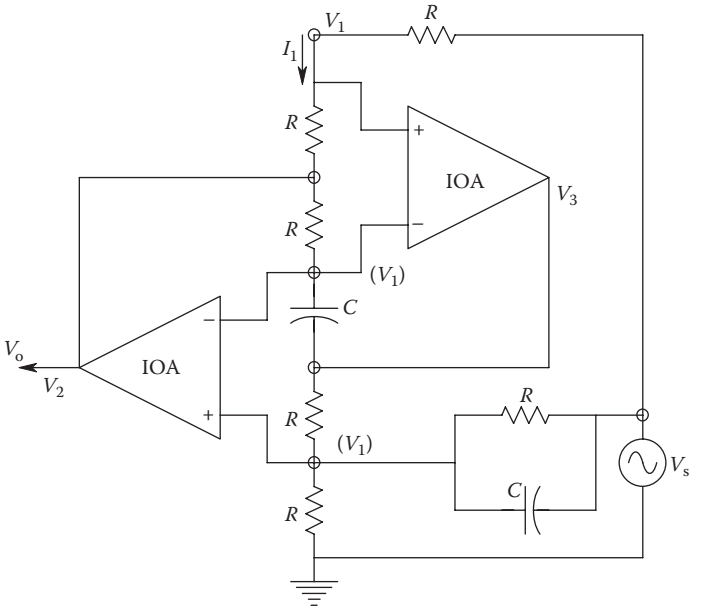


Figure 2.23
A GIC-derived notch filter.

002x023.eps

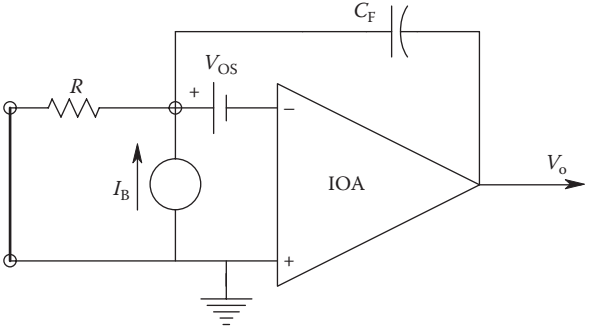


Figure 2.24
An OA integrator circuit showing sources of DC drift error. The magnitudes and signs of the DC bias current, I_B, and the offset voltage, V_{OS}, depend on the particular type of OA used and its temperature.

002x024.eps

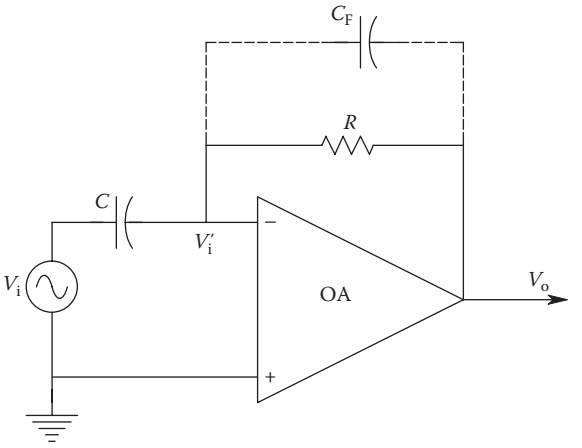


Figure 2.25
A basic OA differentiator. C_F can be used to damp the HF response.

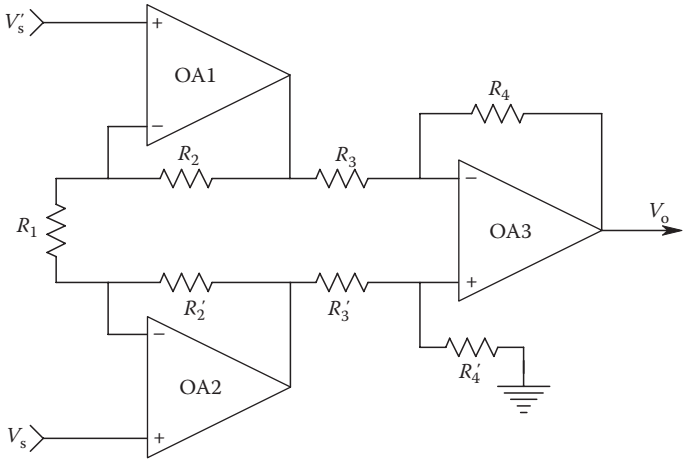


Figure 2.26
Schematic of a three-OA IA.

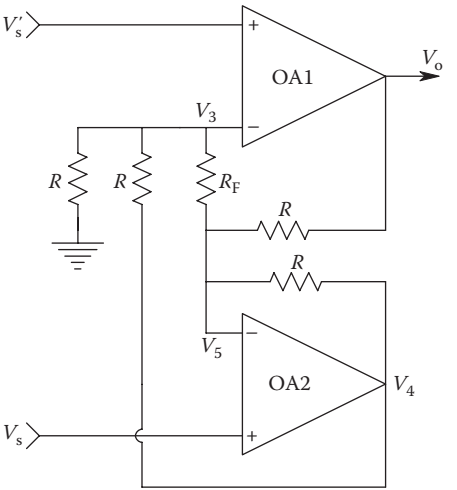


Figure 2.27
A two-OA IA circuit.

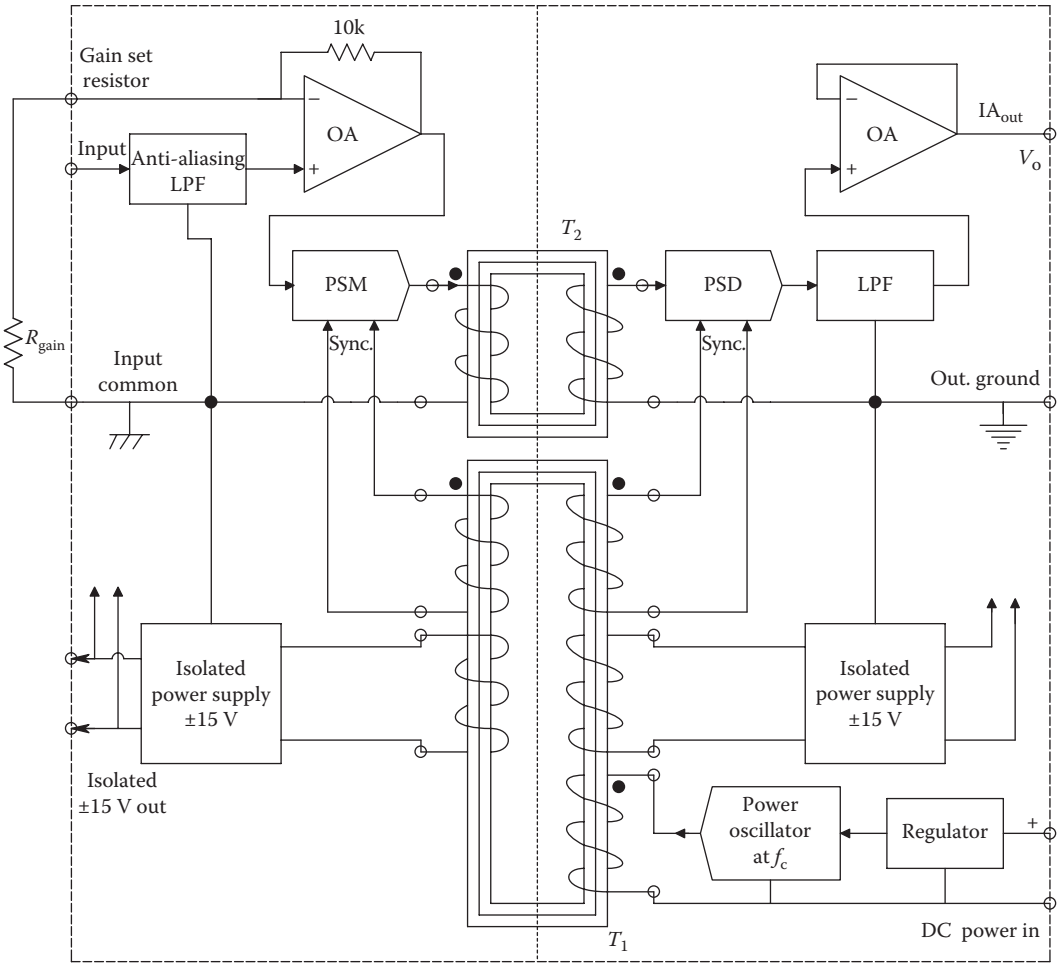


Figure 2.28
A simplified block diagram of an Analog Devices AD295 precision IsoA. (Figure used with permission from Analog Devices.)

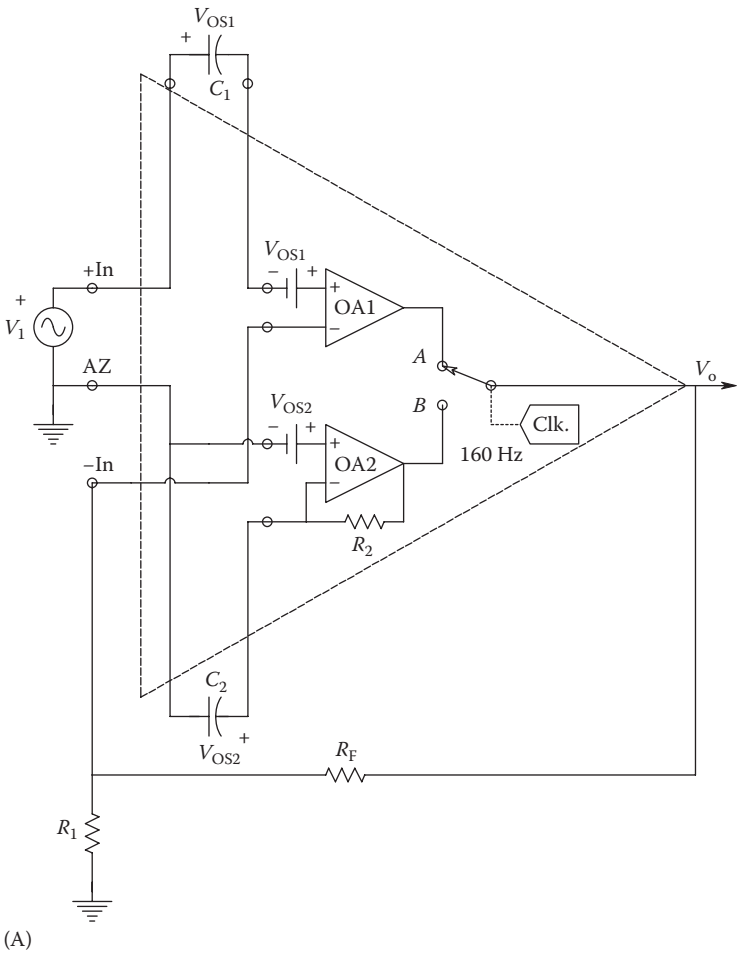


Figure 2.29
(A) Schematic of the innards of an Intersil ICL7605/7606 CAZ amplifier. In this (A) switching cycle, OA1 is connected to the output. OA2 is connected such that its DC offset voltage charges up C_2. C_1 is switched in series with the input node of OA1 so that the voltage on C_1 cancels V_{OS1}.

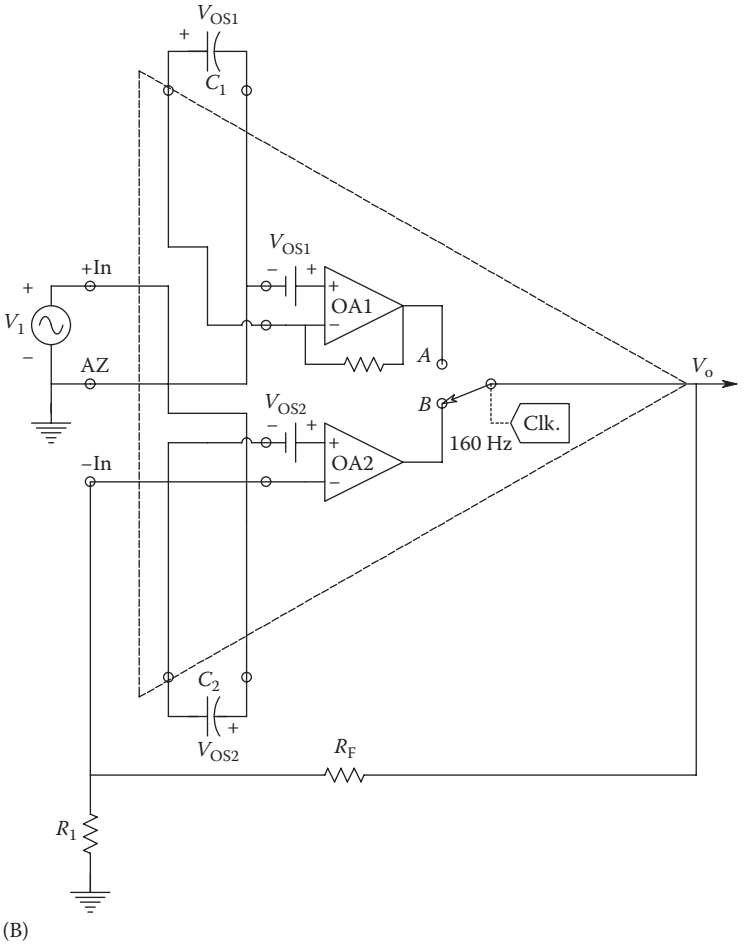


Figure 2.29 (continued)
(B) In the (B) switching cycle, OA2 is connected in series with C_2, so $V_{OS2(k)}$ of OA2 subtracts from $V_{OS2(k-1)}$ on C_2.

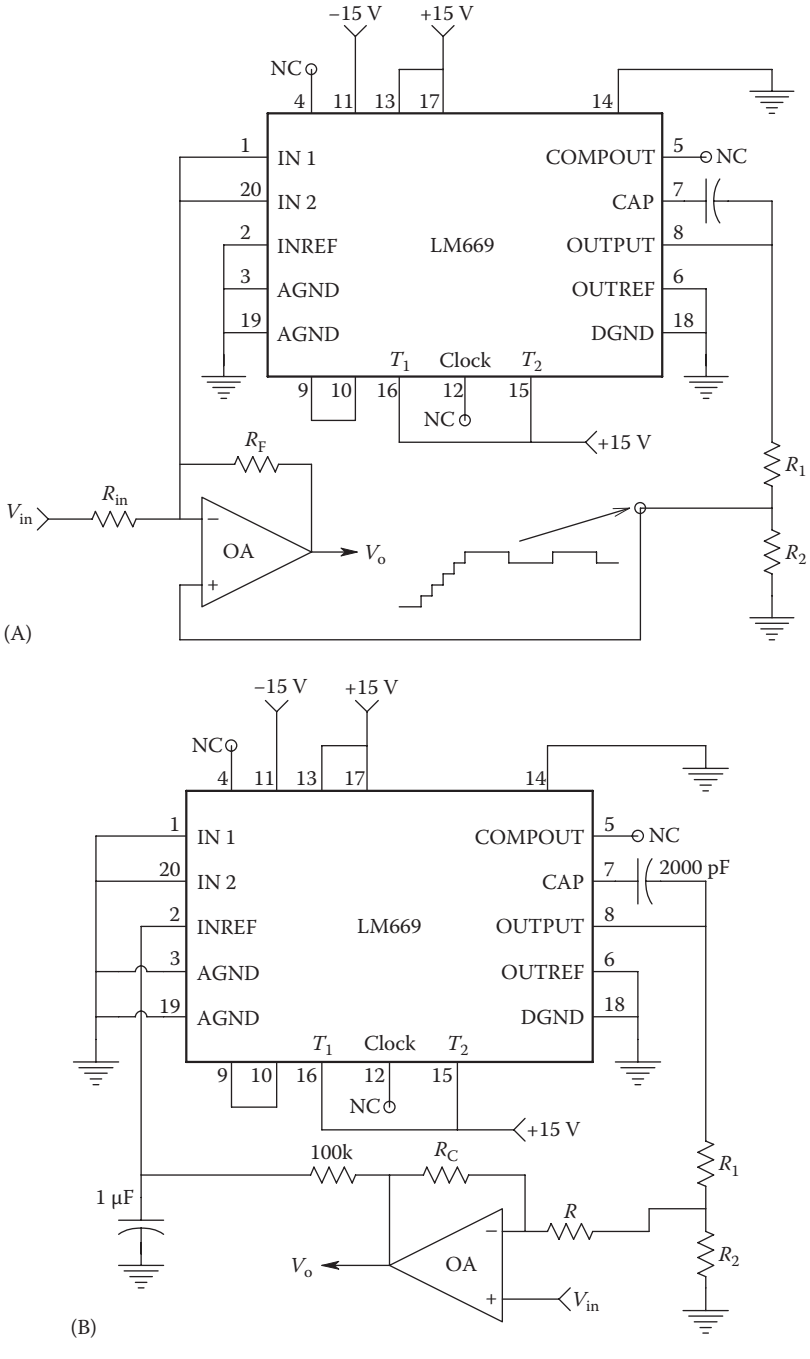


Figure 2.30
(A) The LM669 autozero IC is used to cancel out offset drift in an inverting OA application. The LM669 continually samples the DC voltage at the OA's summing junction and then generates a compensatory DC voltage at the noninverting input. This action nulls the OA's V_{OS} to be effectively ±5 μV. This offset voltage correction compensates for the V_{OS} drift due to temperature and power supply changes. (B) The LM669 acts as a DC servo integrating feedback loop around an OA used as a noninverting amplifier for AC signals. The DC output error of the OA is reduced to about 5 μV, the V_{OS} of the LM669. The LM669 replaces the ground reference for the resistor *R*.

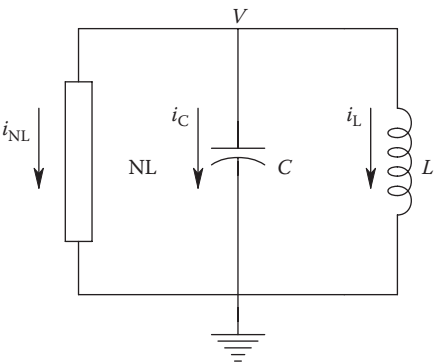


Figure 2.31
A simple nonlinear *RLC* circuit that can be used to illustrate the van der Pol equation for nonlinear oscillations.

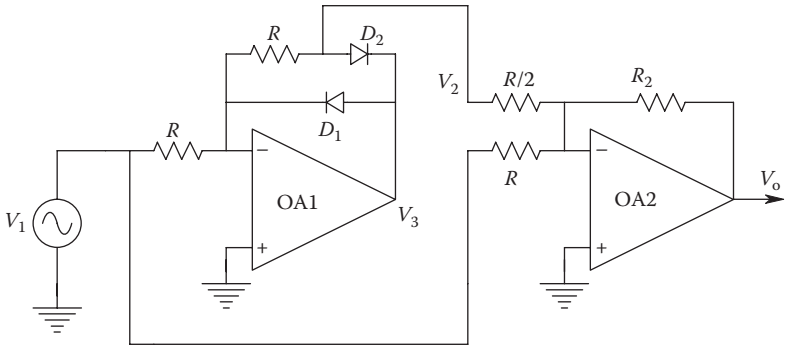


Figure 2.32
A precision, operational, full-wave rectifier or absval circuit.

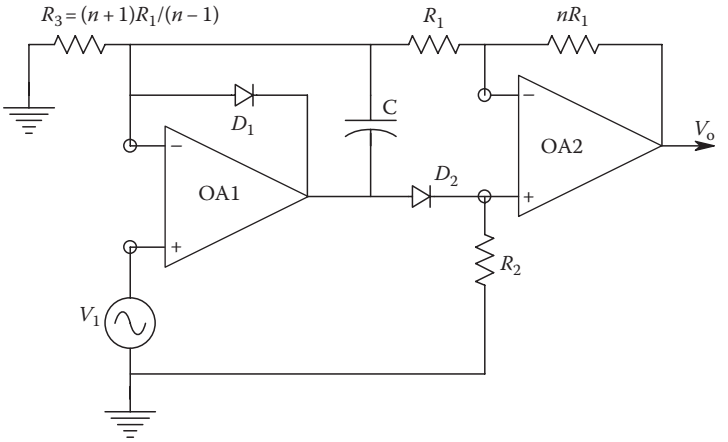


Figure 2.33
A precision absval circuit having high input impedance.

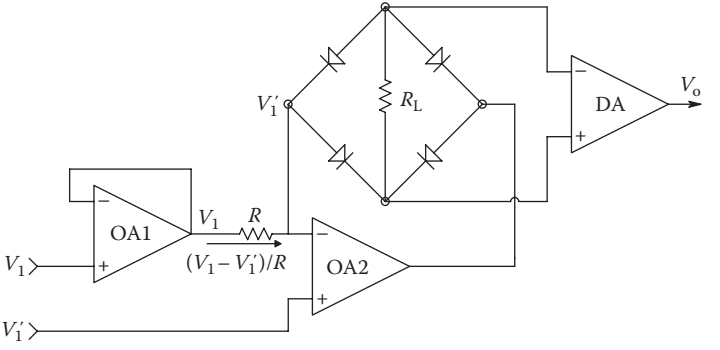


Figure 2.34
A precision absval circuit having a high-impedance, differential input.

002x034.eps

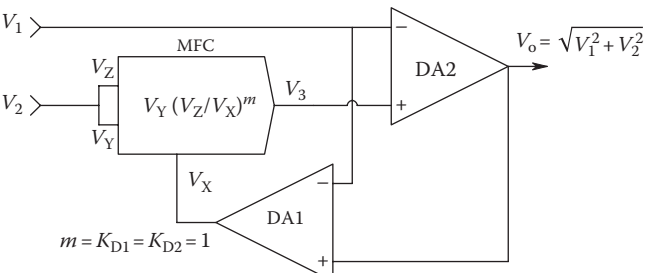


Figure 2.35
A multifunction converter used in a real-time Pythagorean system where $V_o = \sqrt{V_1^2 + V_2^2}$, when $m = K_{D1} = K_{D2} = 1$.

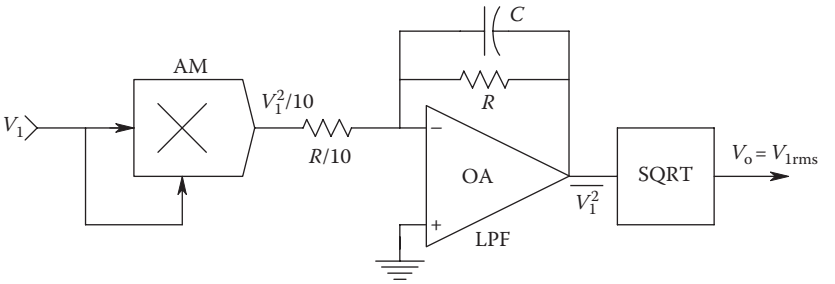


Figure 2.36
Circuit for the generation of the RMS value of an AC signal. The output V_o is a DC voltage.

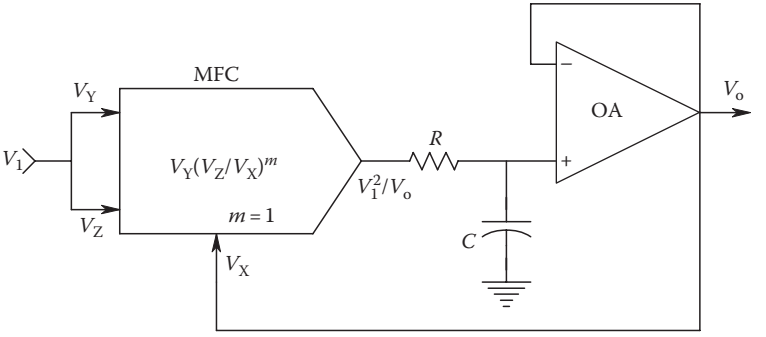


Figure 2.37
In this RMS converter, R and C form an LPF that performs the *mean* operation. A multifunction converter is used in a feedback circuit.

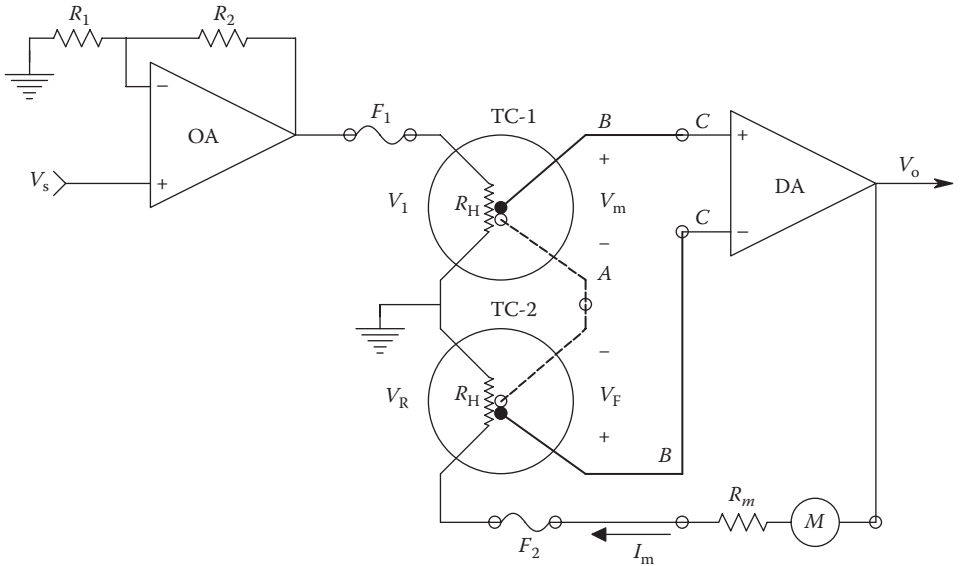


Figure 2.38
Schematic of a simple, feedback-type, true RMS voltmeter using a pair of matched vacuum thermocouples. Fuses F_1 and F_2 protect the delicate thermocouple heaters. I_m is a DC.

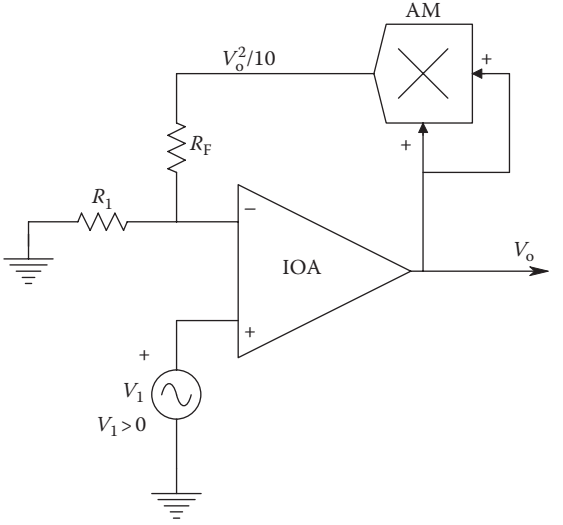


Figure 2.39
A feedback, square-rooting circuit. V_1 must be nonnegative. An analog multiplier IC is used.

002x039.eps

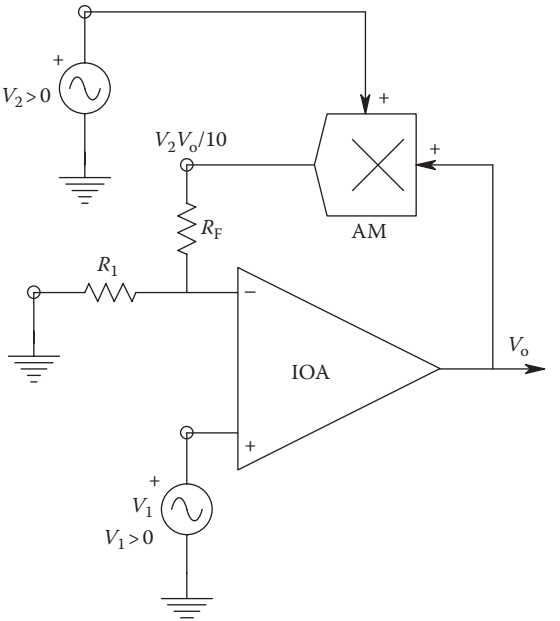


Figure 2.40
The circuit of Figure 2.39 is modified to make an analog divider. Again, V_1 must be nonnegative, and V_2 must be positive and greater than $V_{2MIN} = (V_{1MIN}/V_{OSat})(10R_F/R_1)$ to prevent OA output saturation and also less than the supply voltage of the OA (e.g., +15 V) to avoid damaging the OA's input transistors.

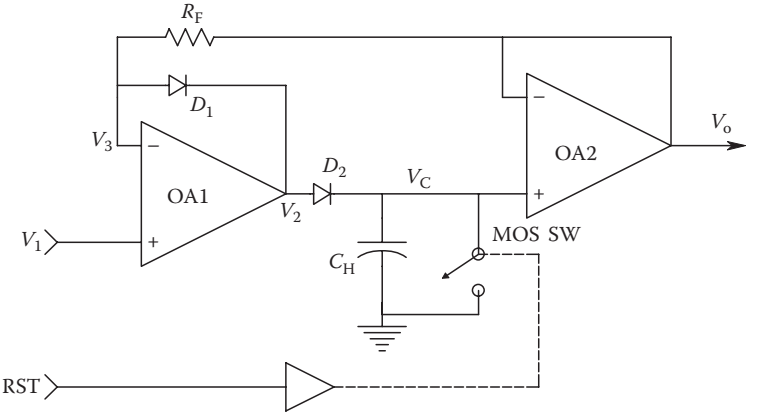


Figure 2.41
A MOSFET switch, SW1, is used to reset the two-OA peak detector.

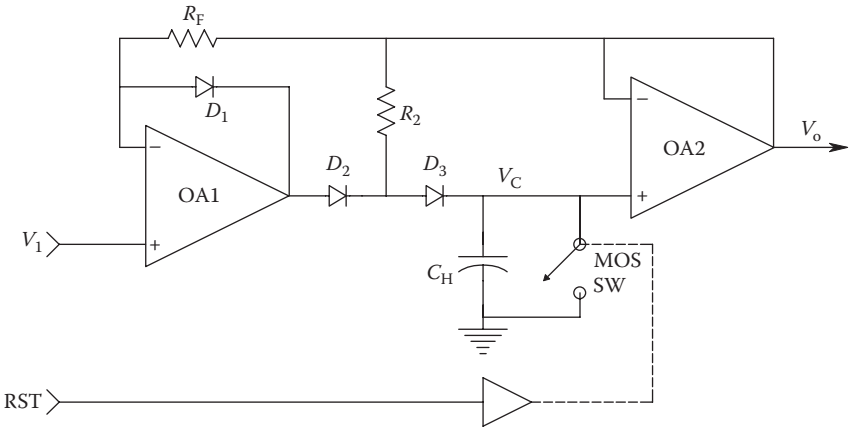


Figure 2.42
An improved peak detector design.

002x042.eps

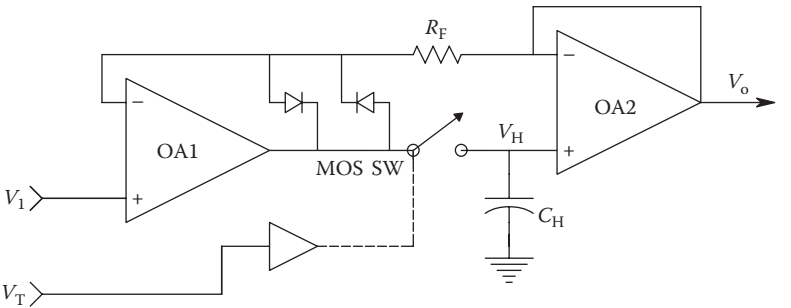


Figure 2.43
A basic, unity-gain, T&H circuit.

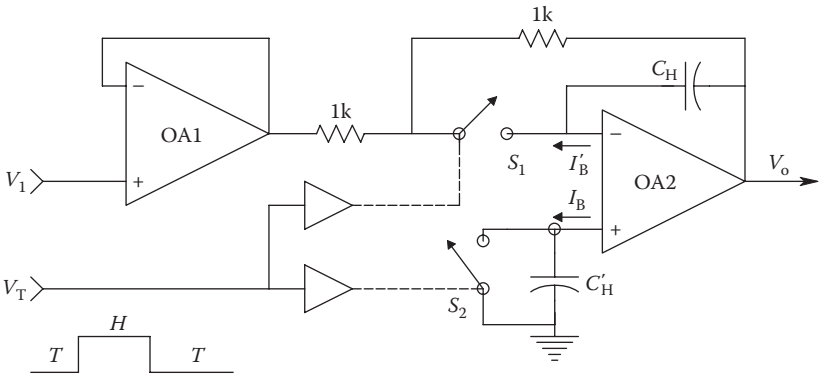


Figure 2.44
Basic architecture of the Burr-Brown SHC803BM T&H circuit. S_2 and capacitor C'_H are used for cancelation of the pedestal voltage.

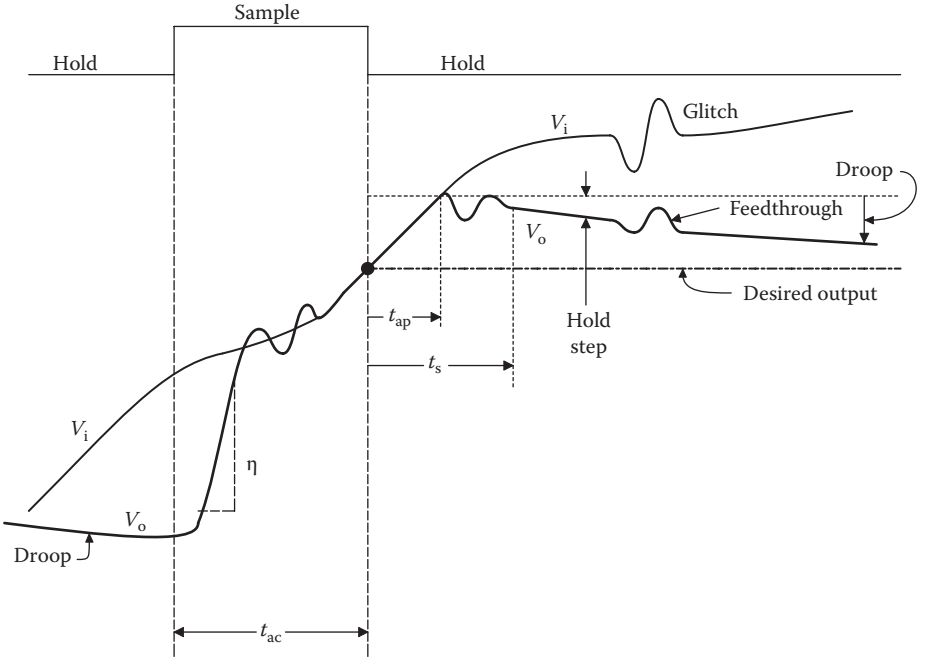


Figure 2.45
Waveforms seen in the operation of a typical T&H circuit. (From Franco, S., *Design with Operational Amplifiers and Integrated Circuits*, McGraw-Hill Book Co., New York, 1988. With permission.)

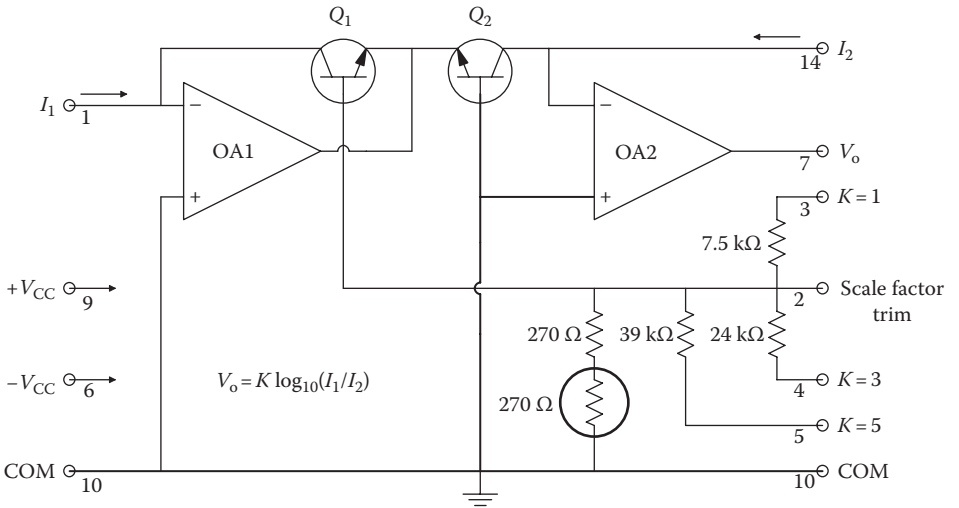


Figure 2.46
Simplified schematic of the Burr-Brown LOG100 log ratio converter. (Courtesy of Burr-Brown, Tucson, AZ.)

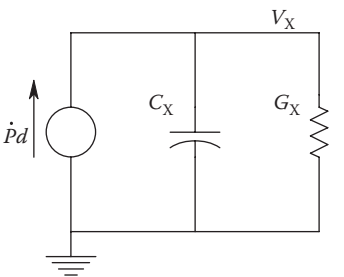


Figure 2.47
Equivalent circuit of a piezoelectric crystal responding to pressure on its active surface at frequencies well below its mechanical resonance frequency.

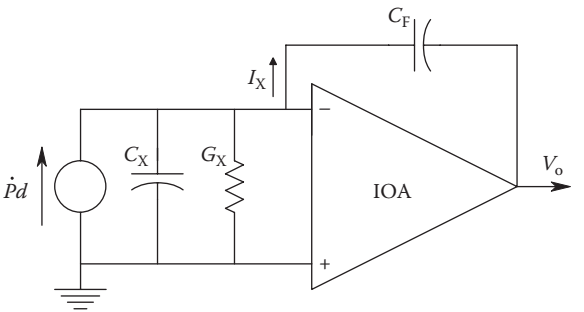


Figure 2.48
A charge amplifier circuit used to condition the output of a piezoelectric crystal sensor.

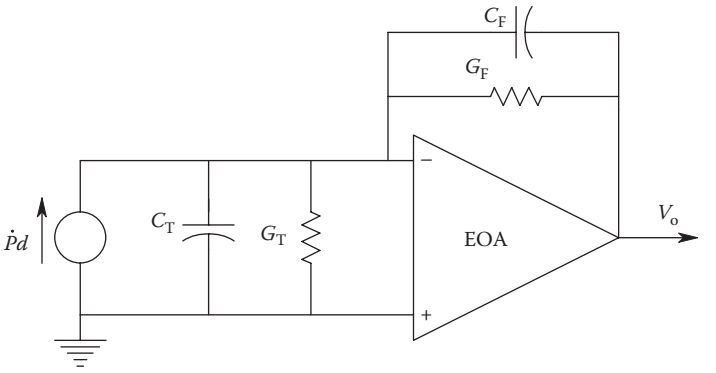


Figure 2.49
Circuit of a practical charge amplifier and crystal sensor.

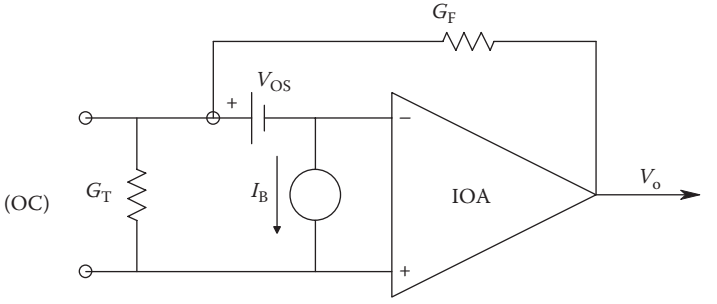


Figure 2.50
The DC equivalent circuit of a practical charge amplifier. V_{OS} = DC offset voltage, I_B = DC input bias current.

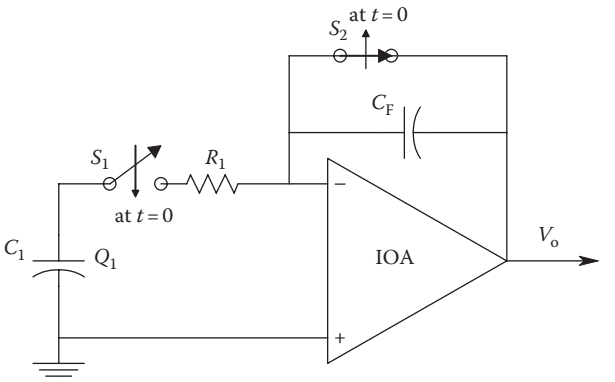


Figure 2.51
An integrating coulombmeter circuit. An EOA is generally used.

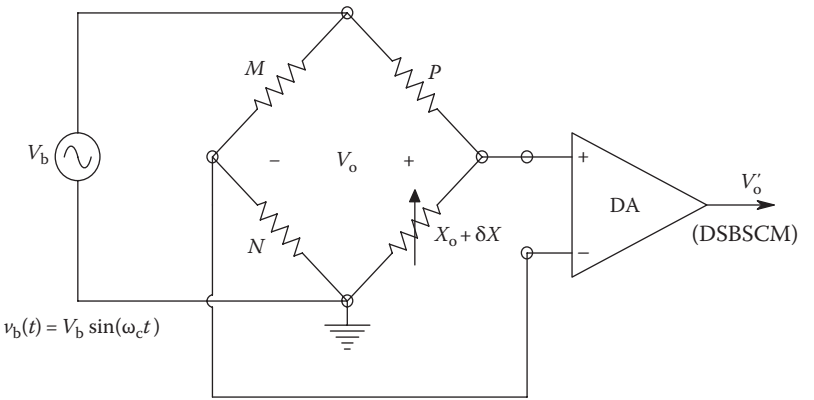


Figure 2.52
A Wheatstone bridge circuit with AC excitation generates a DSBSCM output.

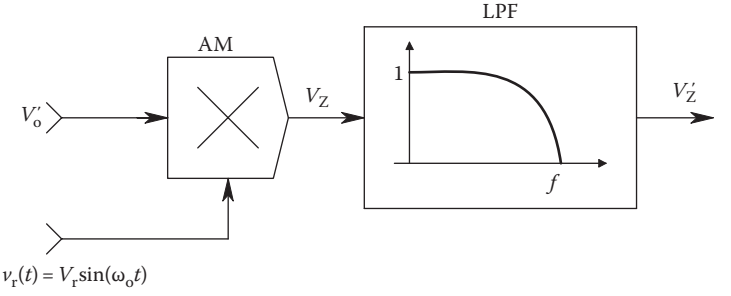


Figure 2.53
An analog multiplier followed by an LPF is used to demodulate a DSBSCM signal.

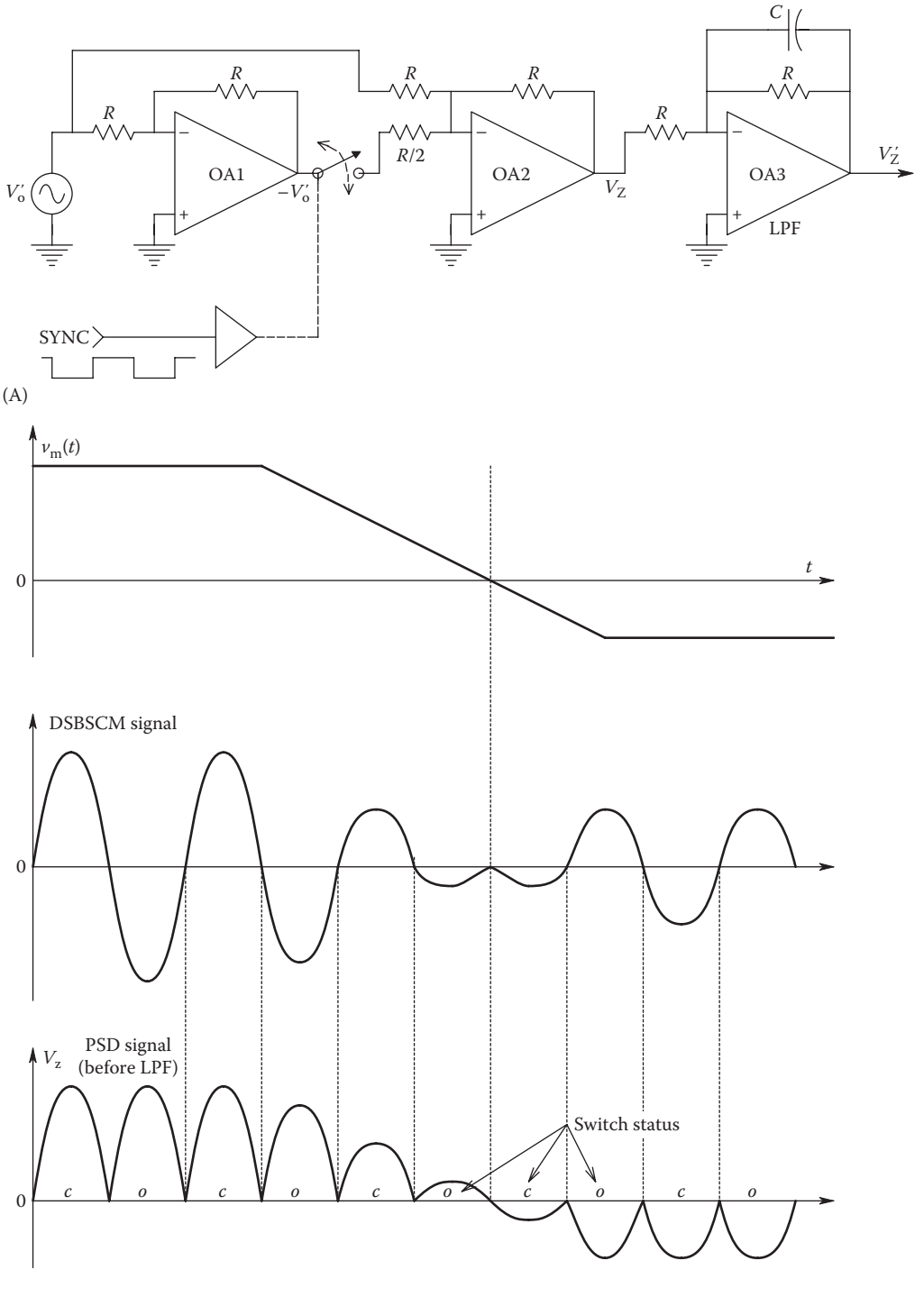


Figure 2.54
(A) A simple PSR and LPF circuit using OAs and a MOS switch. (B) Waveforms in the PSR/LPF circuit.

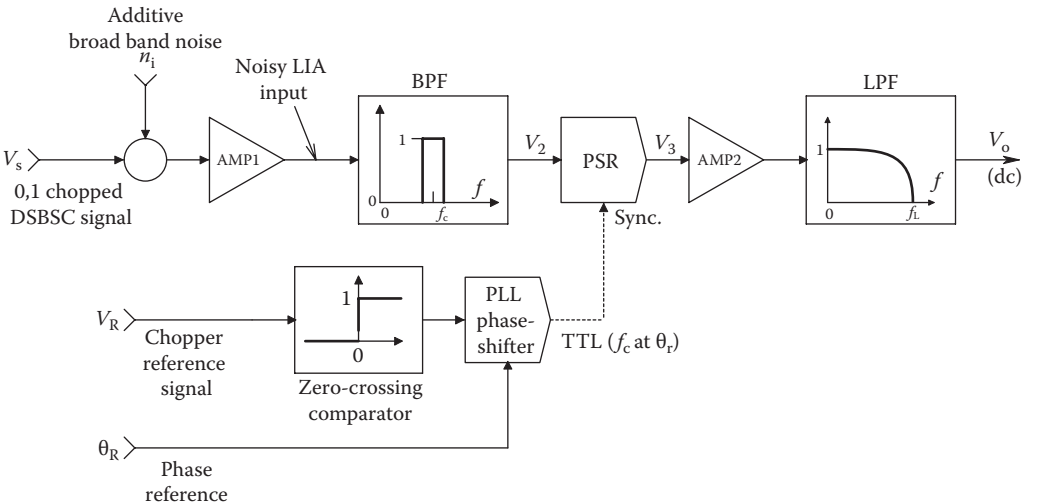


Figure 2.55
Block diagram of an LIA. Input is a 0,1 chopped, noisy signal, such as the output of a photosensor. Amplification and BP filtering at the chopper frequency converts the input signal into a noisy AC signal, which is then rectified by the PSR. The LF modulating signal is seen at the LIA output. The LPF bandwidth is adjusted to pass the desired modulating signal with the least amount of noise.

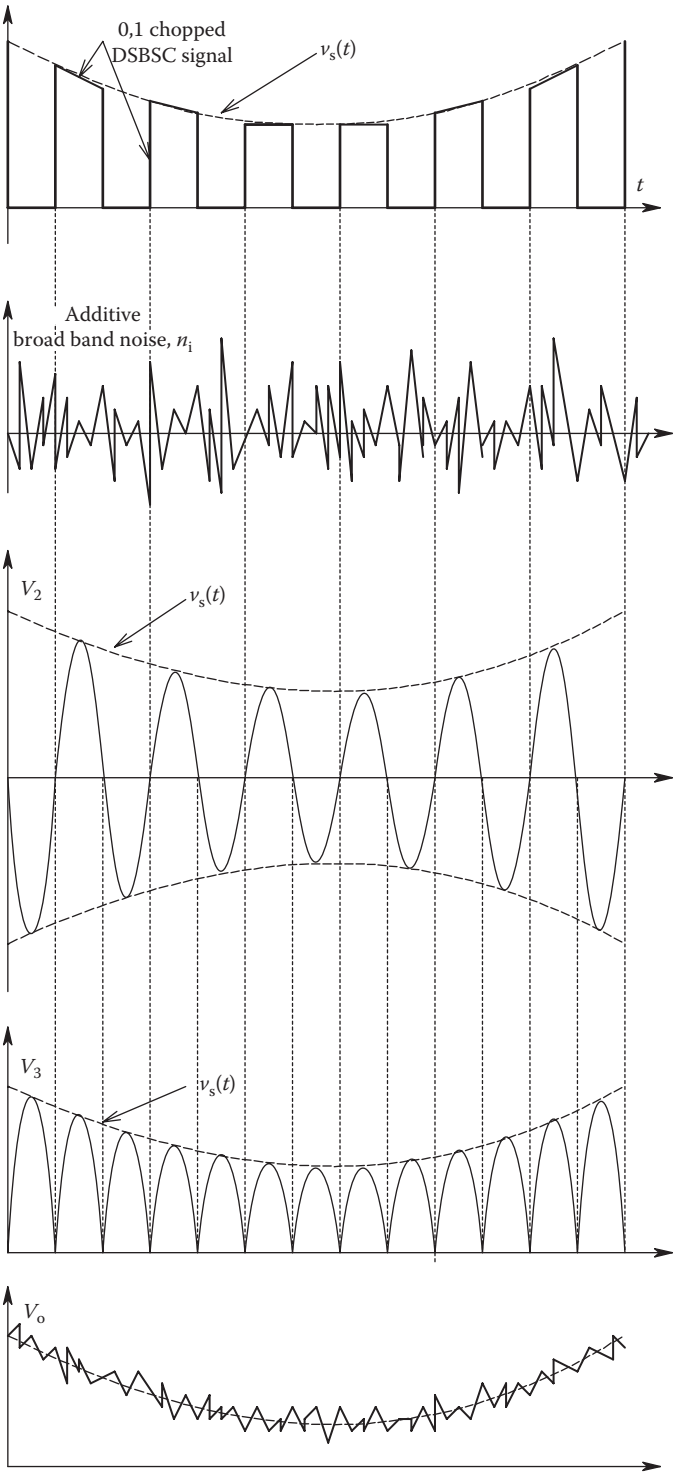


Figure 2.56
Waveforms in the LIA of Figure 2.55.

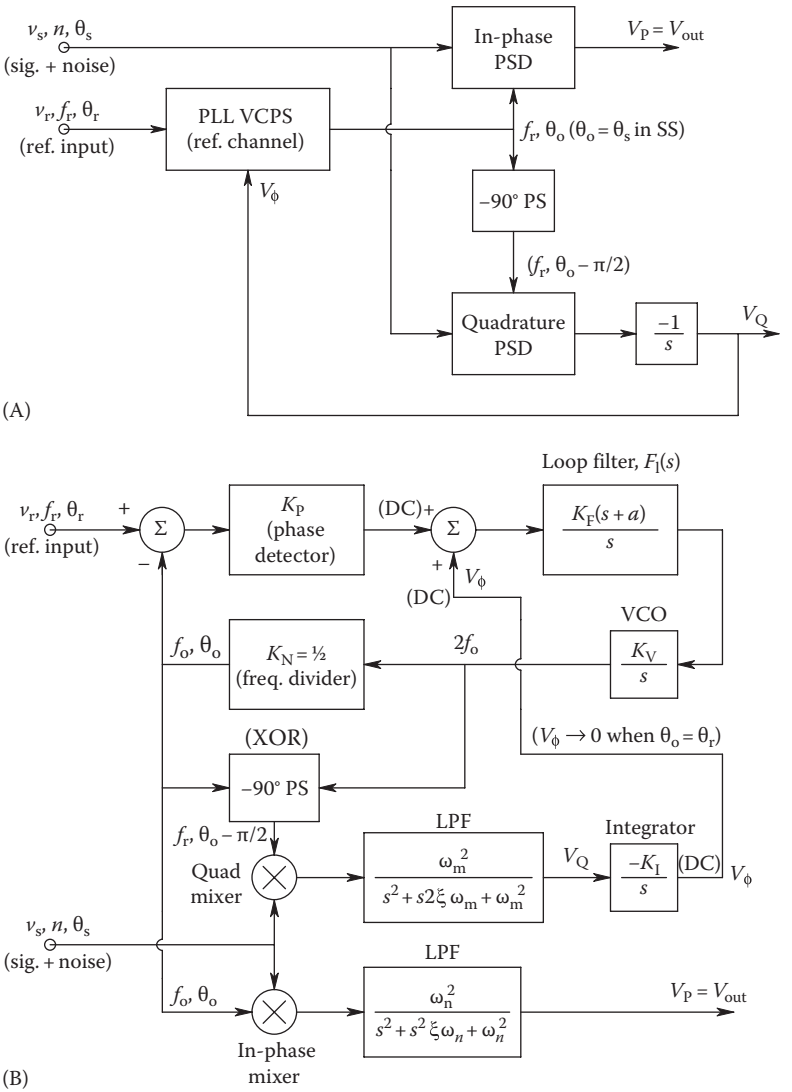


Figure 2.57
(A) Block diagram of McDonald's vector-tracking LIA. (B) Functional block diagram of McDonald's vector LIA.

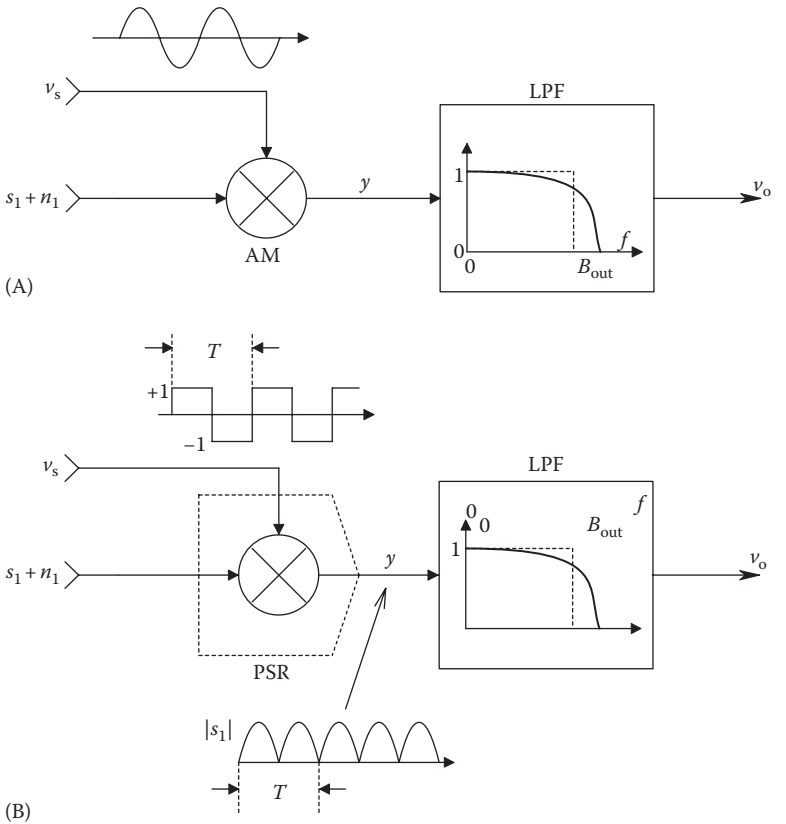


Figure 2.58
Two means of demodulating DSBSCM signals used in LIAs. (A) Demodulation by analog multiplier and LPF. (B) Demodulation by synchronous rectifier and LPF.

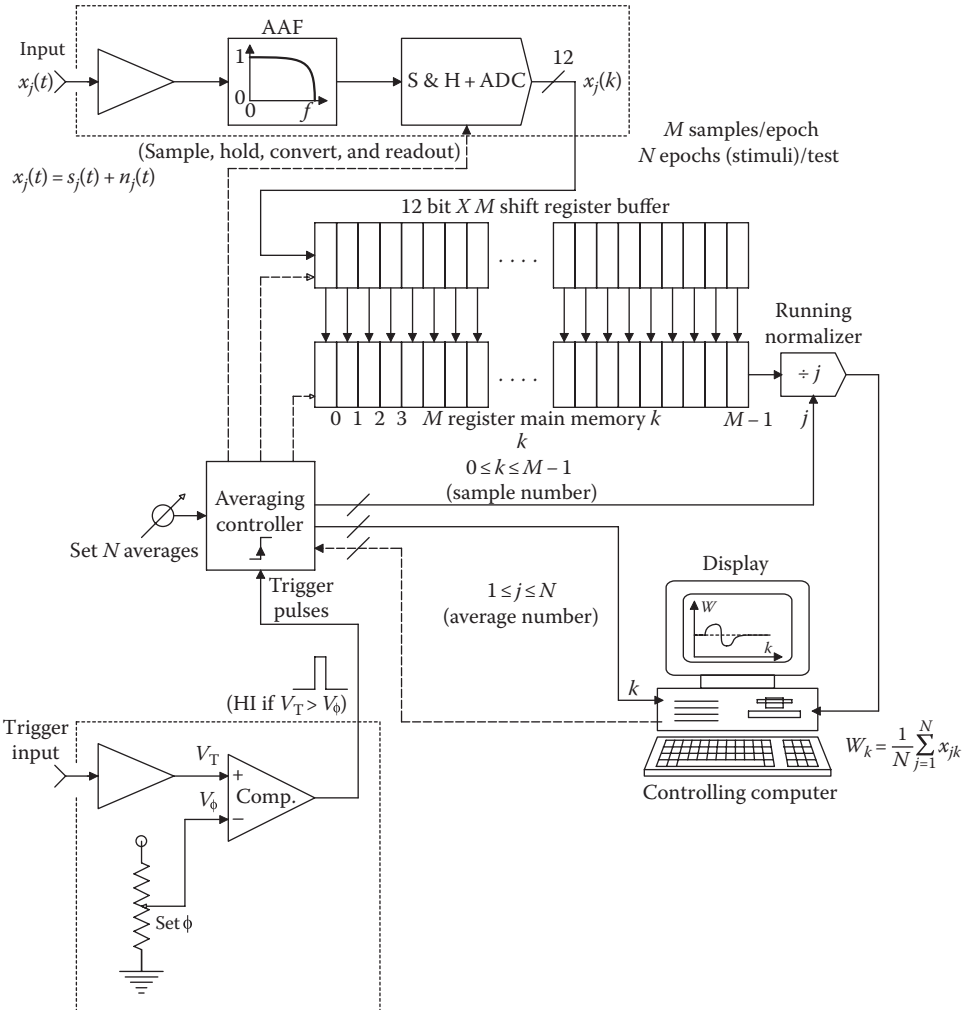


Figure 2.59
Organizational block diagram of a synchronous signal averager. The trigger input and signal digitizer (inside dotted lines) are typically on an accessory card; the registers and averaging controller typically exist as software operations inside the computer.

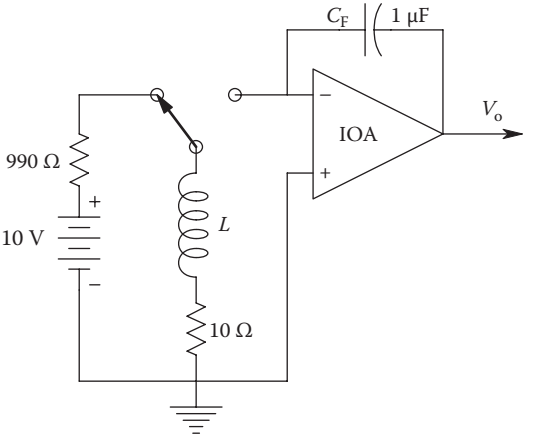


Figure P2.1

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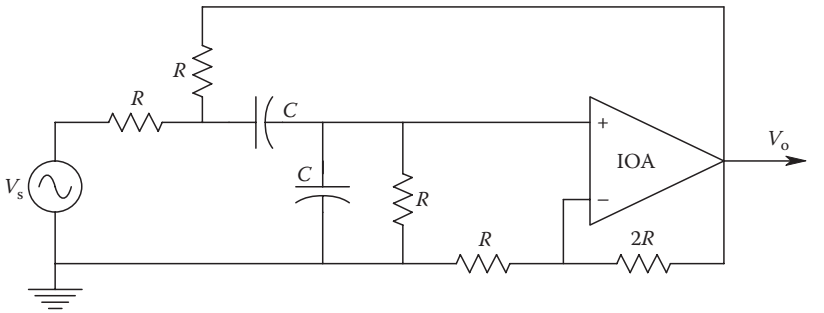

Figure P2.2

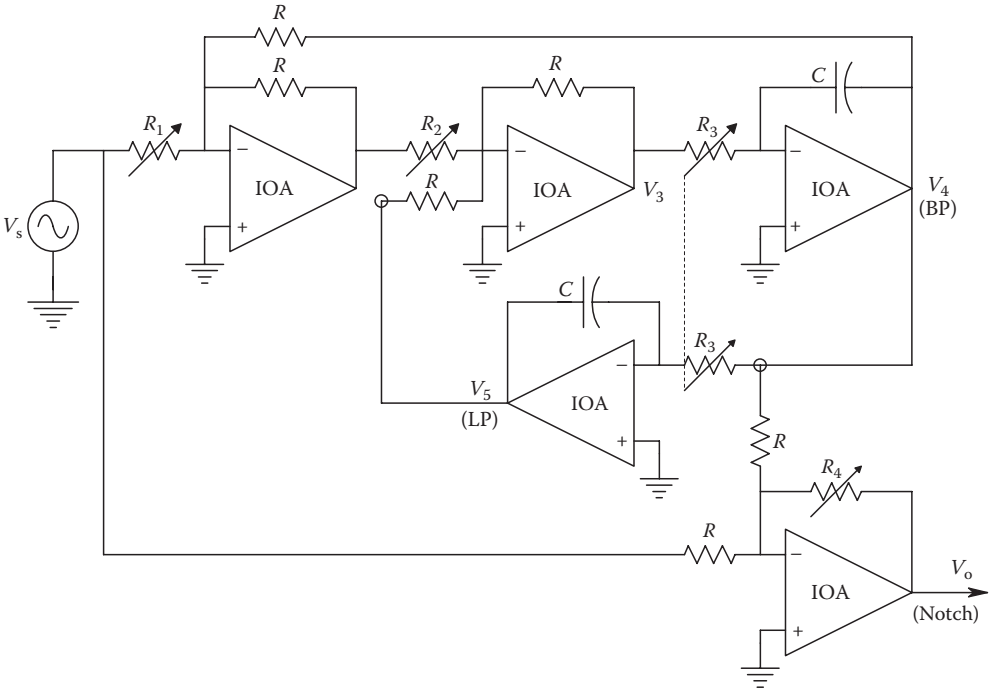

Figure P2.3

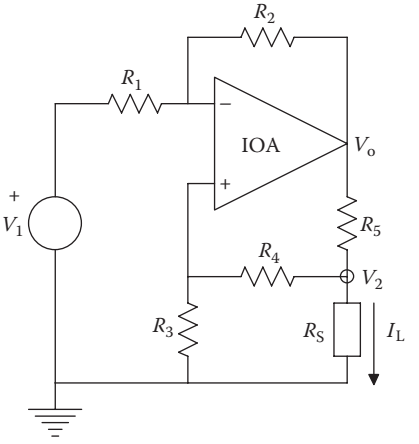

Figure P2.4

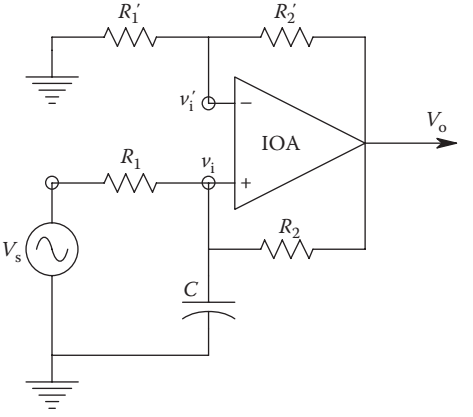

Figure P2.5

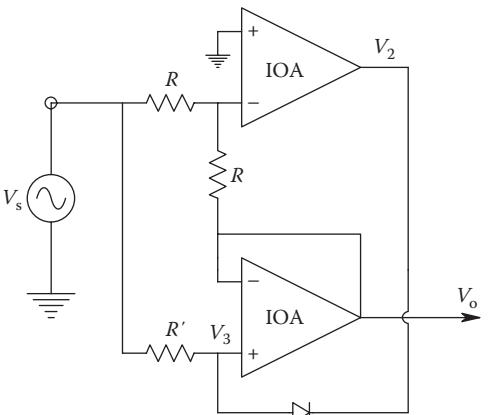

Figure P2.6

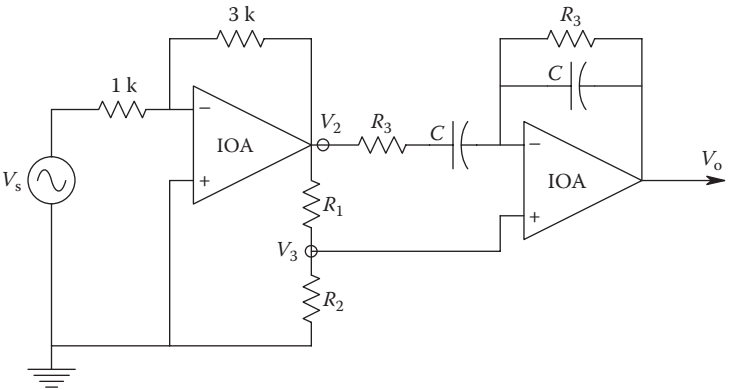

Figure P2.7

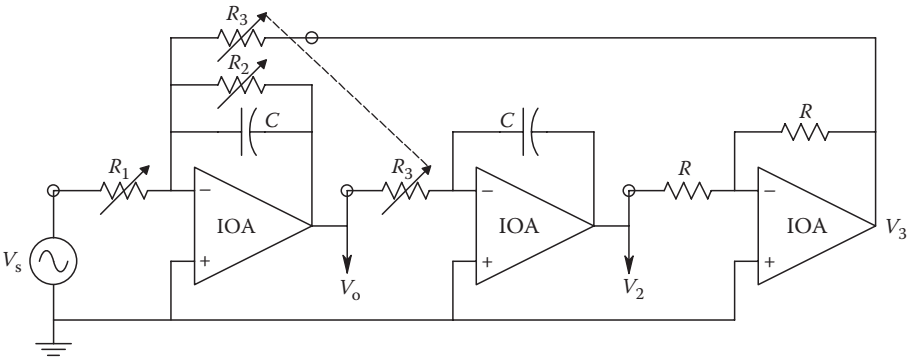

Figure P2.8

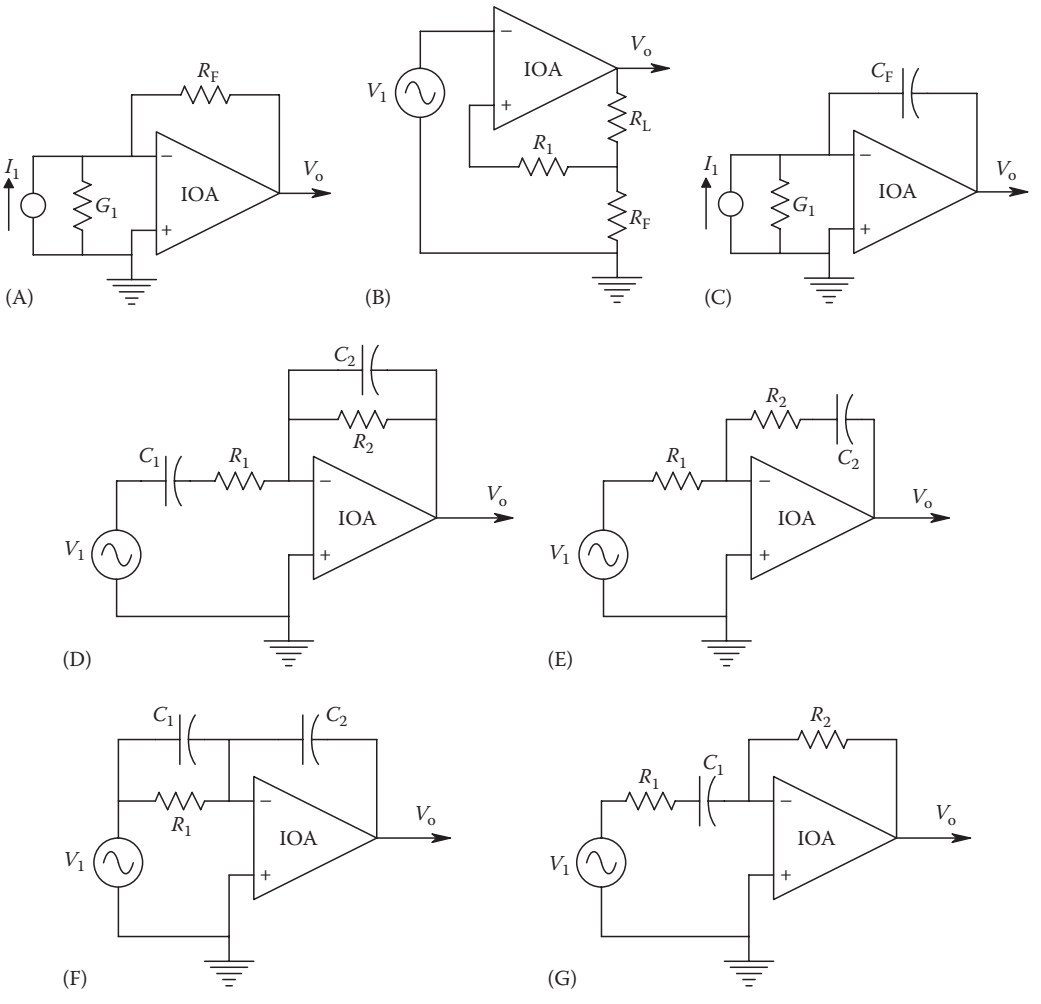

Figure P2.9

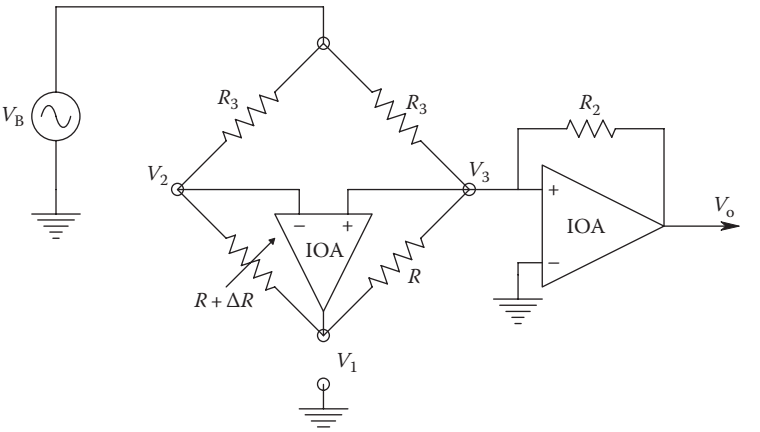

Figure P2.10

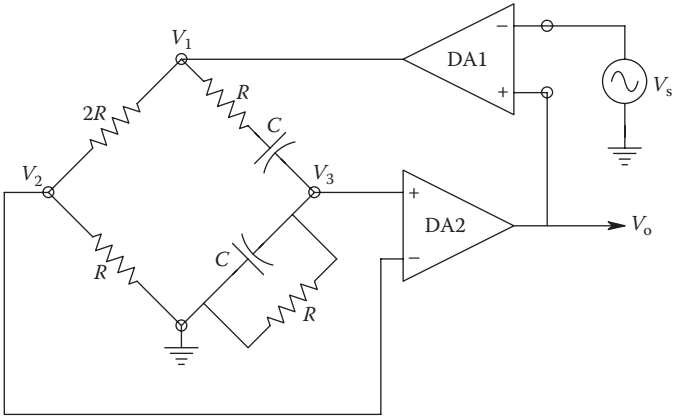

Figure P2.13

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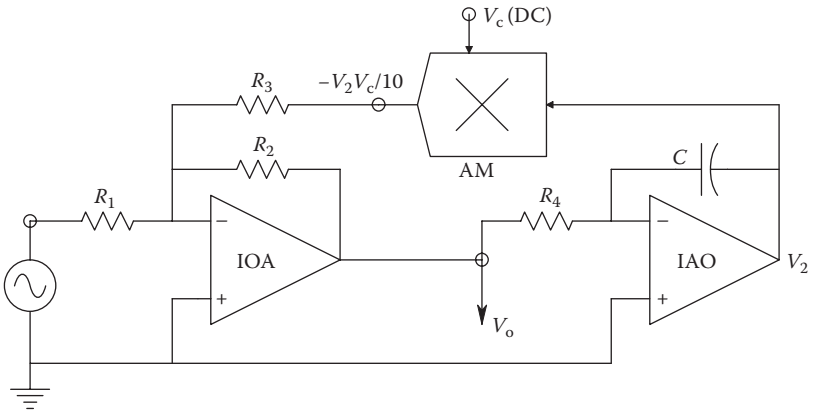

Figure P2.15

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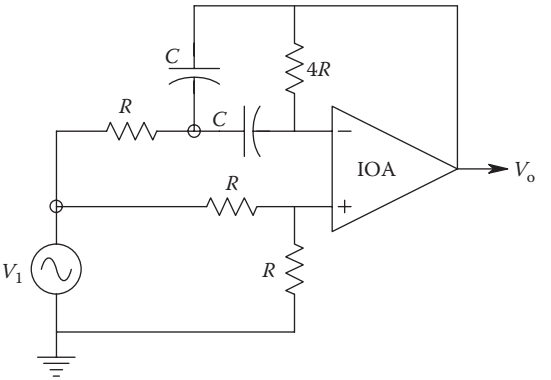

Figure P2.16

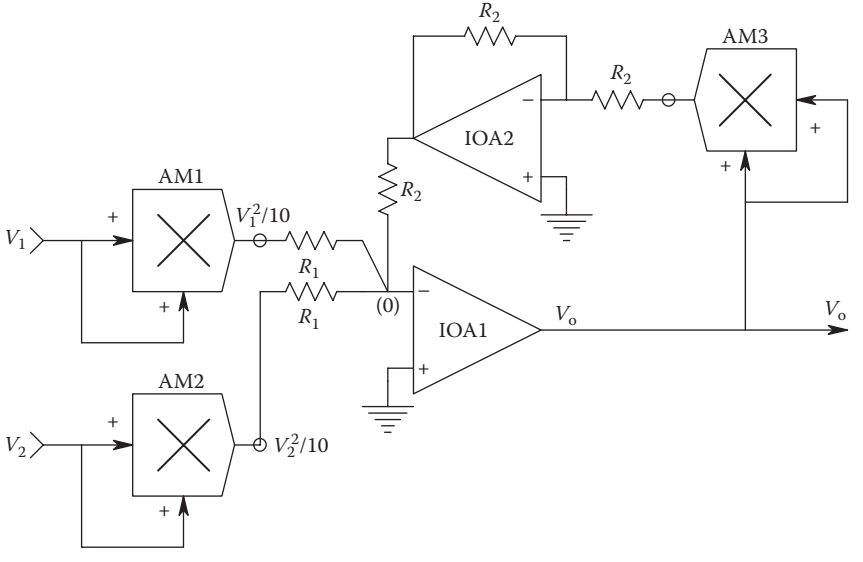

Figure P2.17

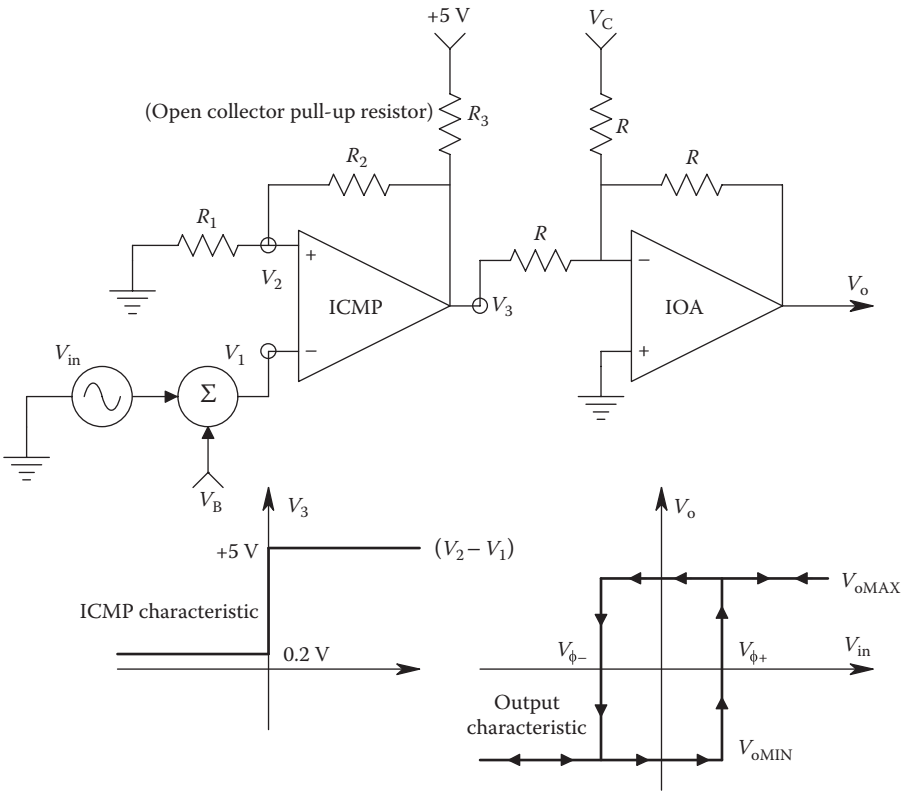

Figure P2.18