FIGURE 2.1

IPOS cycle.

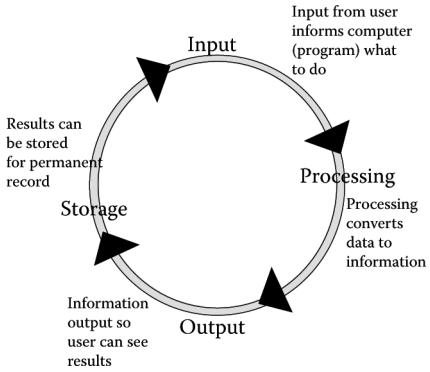


FIGURE 2.2

Structure of modern computers.

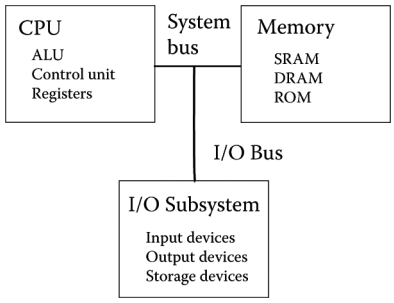


FIGURE 2.3

System bus connecting CPU and memory.

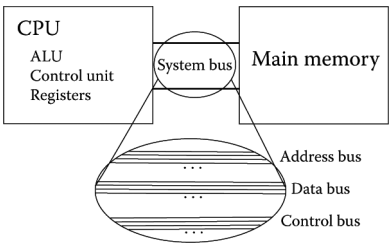
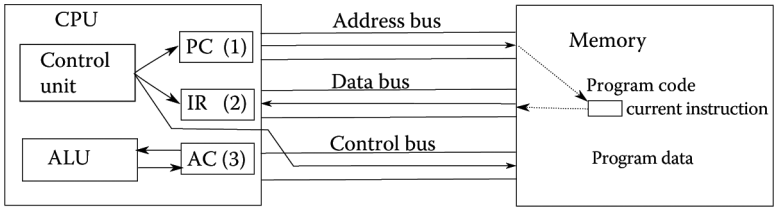


FIGURE 2.4

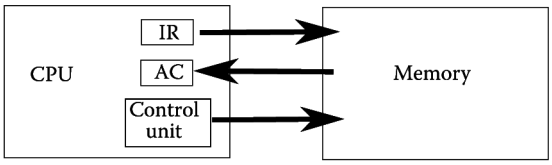
Three-part fetch–execute cycle.



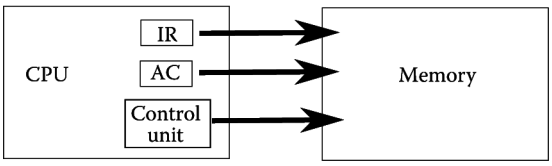
1. Control unit moves PC to address bus and signals memory "read" command over control bus, memory returns instruction over data bus to be stored in IR
2. Control unit decodes instruction in IR
3. Execute instruction in the ALU using datum in AC, putting result back in the AC

FIGURE 2.5

Memory read (top) versus memory write (bottom).



1. Address from IR to address bus
   control unit signals memory read
   over control bus
2. Memory accesses address
   returns datum over data bus
3. Datum stored in AC



1. Address from IR to address bus
   datum from AC over data bus
   control unit signals memory write
   over control bus
2. Memory accesses address
   stores datum from data bus to
   memory location

FIGURE 2.6

Improvement in CPU speed over memory access time.

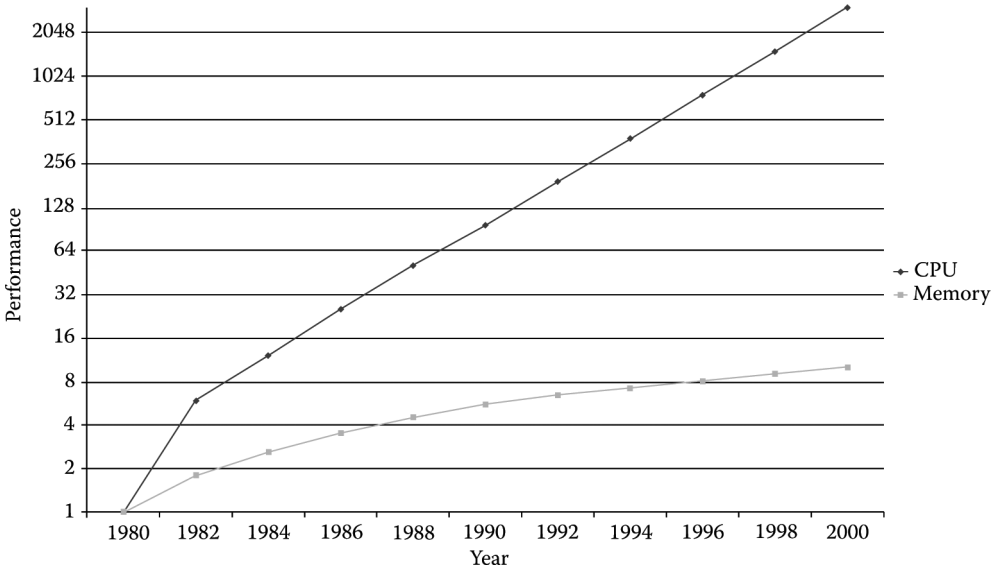


FIGURE 2.7

Memory hierarchy.

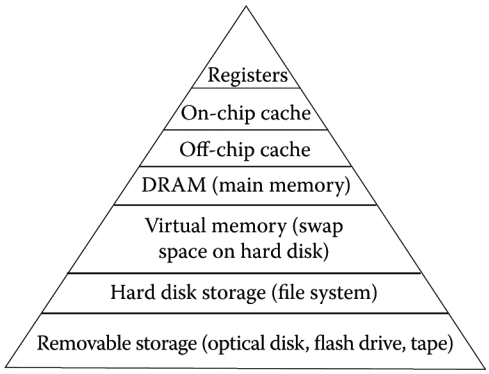


FIGURE 2.8

Virtual reality headset and data glove in use. (Courtesy of NASA, http://gimp-savvy.com/cgi-bin/img.cgi?ailsxmzVhD8OjEo694.)