Lecture 02: Ratioless Logic Designs

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Syllabus

- Basic operations of switches
- Switch logic circuits
- Systematic design methodologies

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- Basic operations of switches
  - nMOS switches
  - pMOS switches
  - TG switches
  - Basic logic circuits
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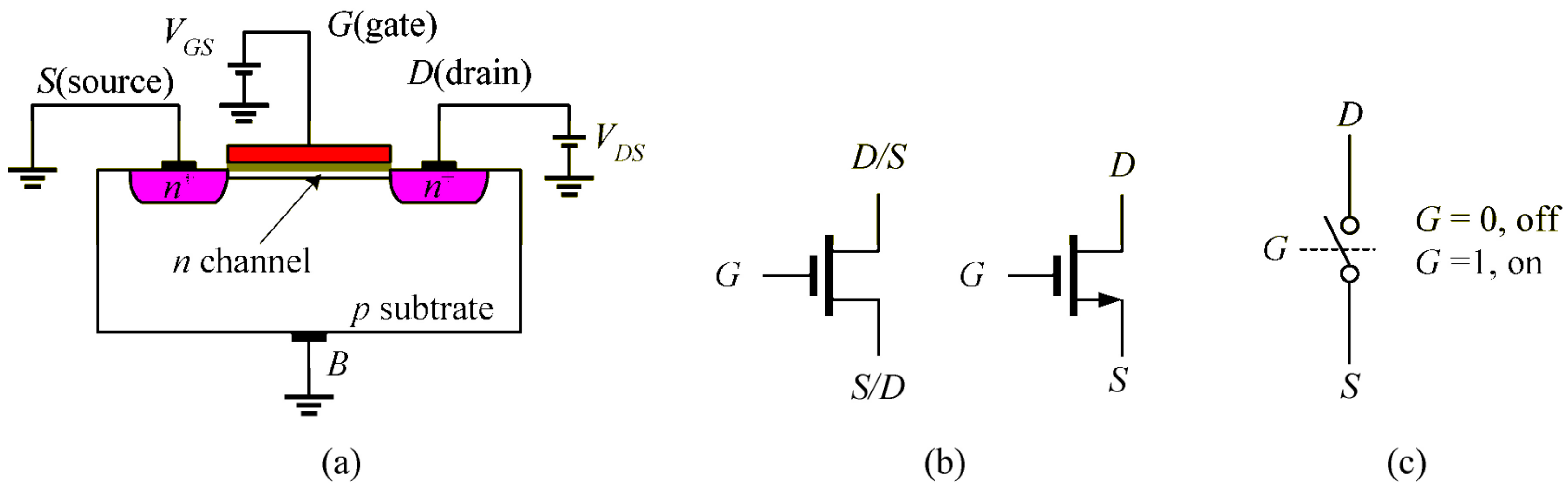
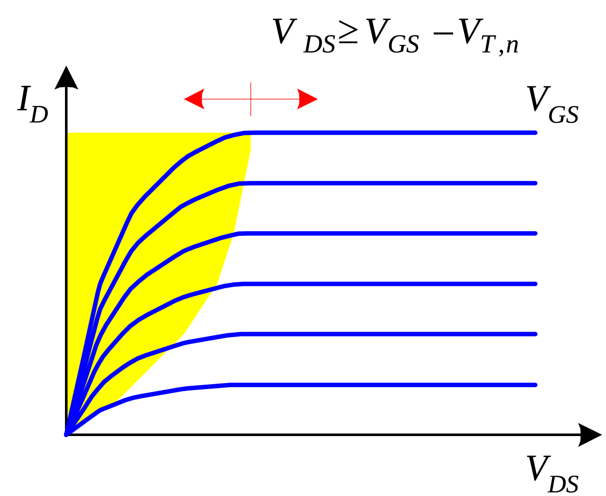
nMOS Switches

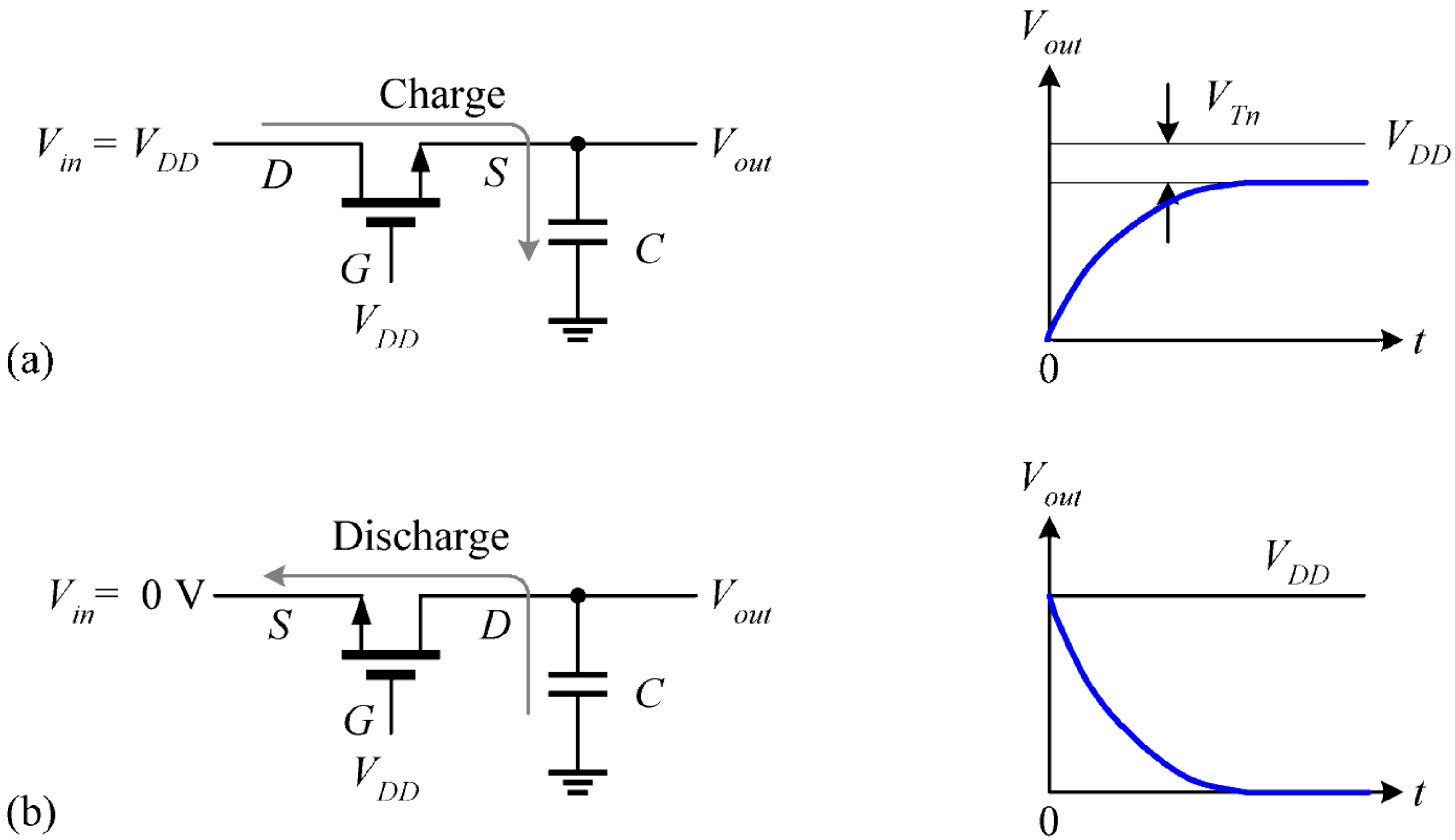


$$I_D = \mu_n C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_{T,n} - \frac{1}{2} V_{DS} \right) V_{DS} \right]$$

$$I_{D,sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{T,n} \right)^2$$



nMOS Switches



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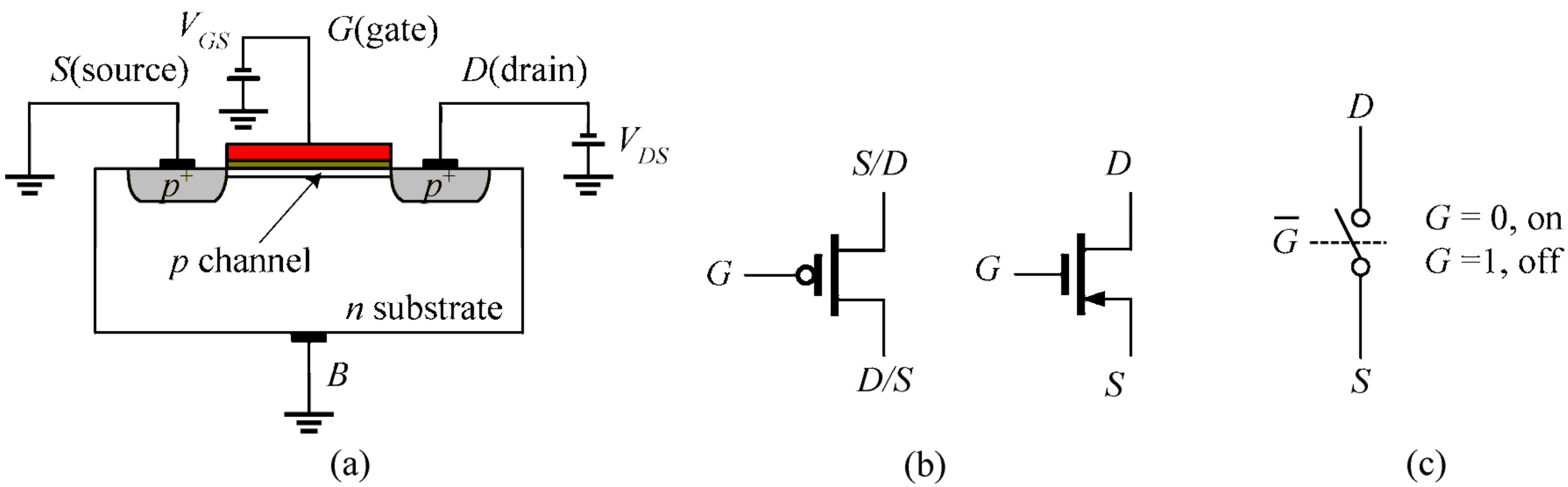
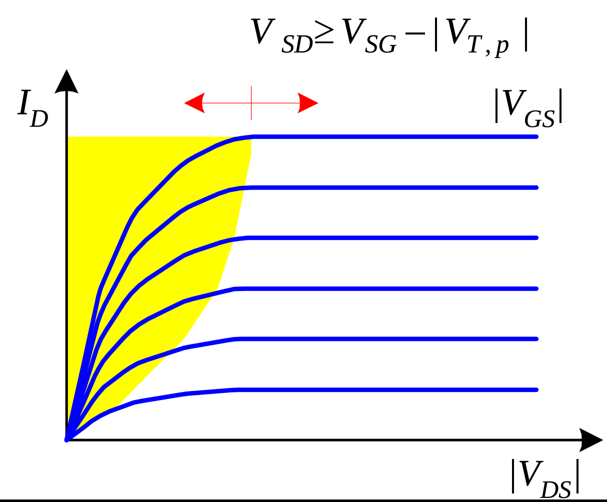
pMOS Switches

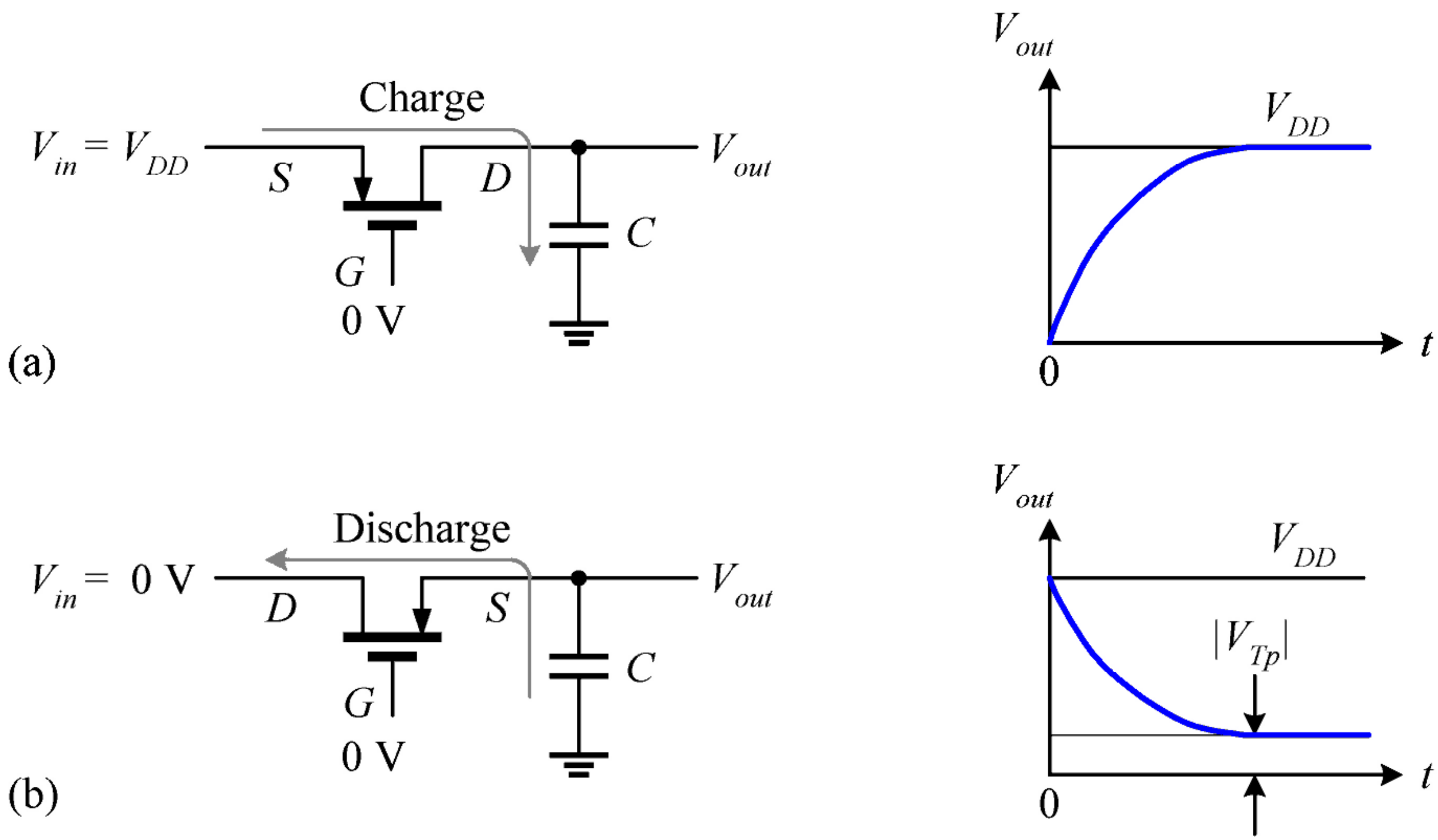


$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{SG} - |V_{T,p}| - \frac{1}{2}V_{SD}\right)V_{SD}\right]$$

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{SG} - |V_{T,p}|\right)^2$$



pMOS Switches



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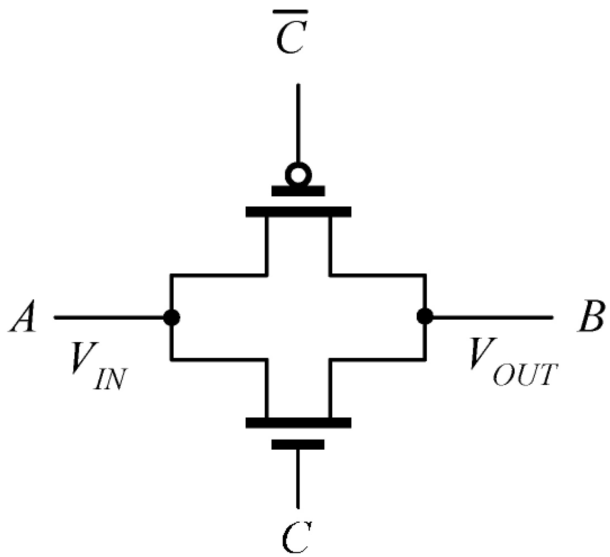
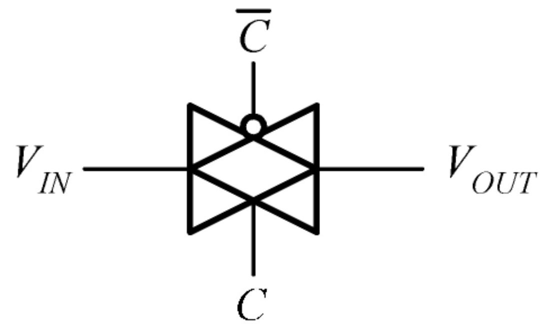
TG Switches

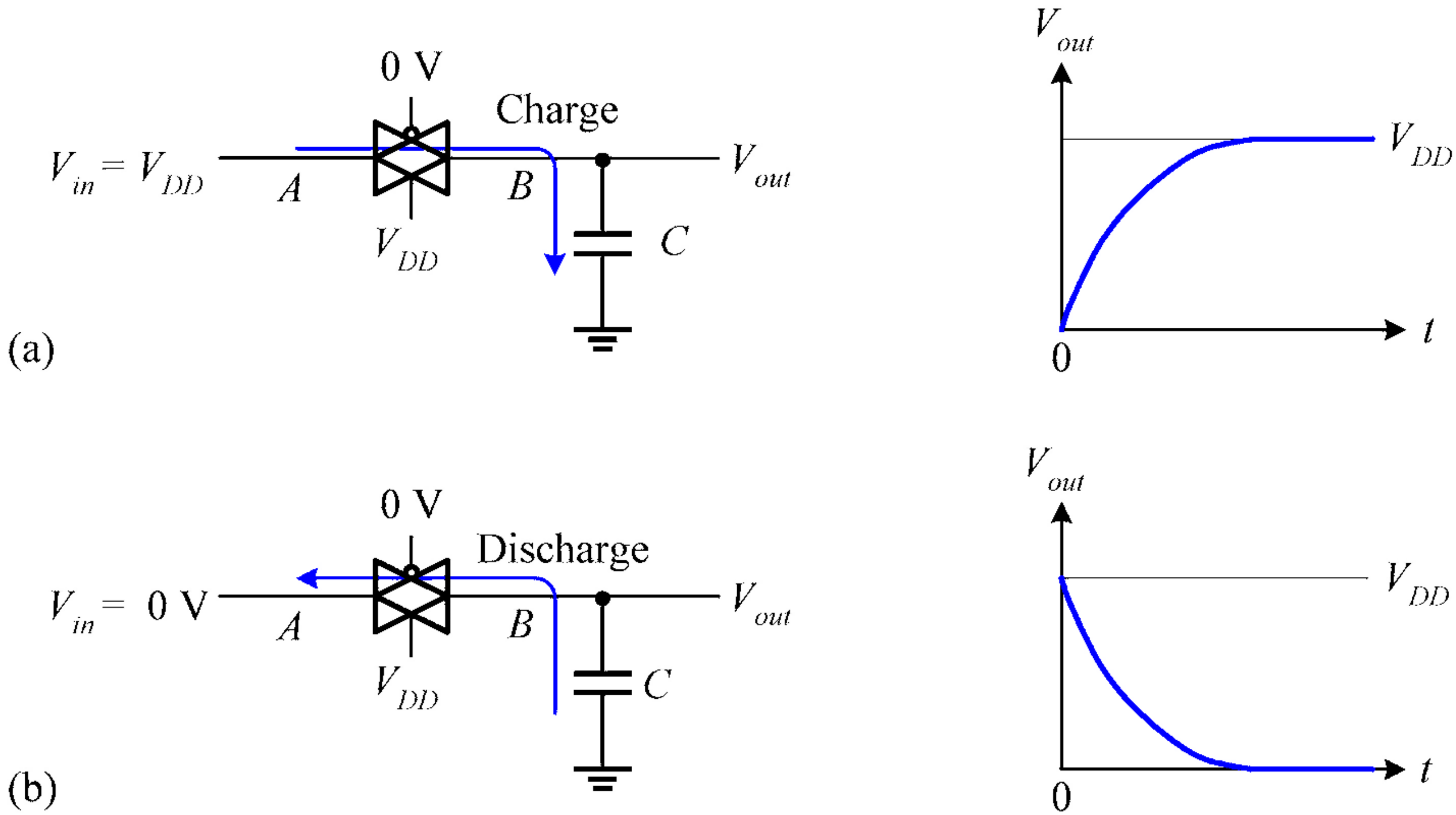


(a)



(b)

TG Switches


0 V
Charge
$V_{in} = V_{DD}$
A
B
V_{out}
V_{DD}
C
(a)
V_{out}
V_{DD}
t
0
0 V
Discharge
$V_{in} =$ 0 V
A
B
V_{out}
V_{DD}
C
(b)
V_{out}
V_{DD}
t
0

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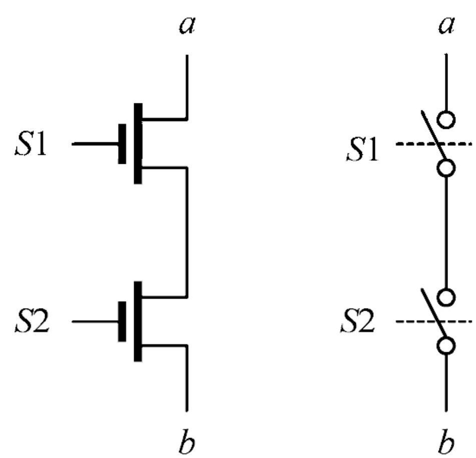
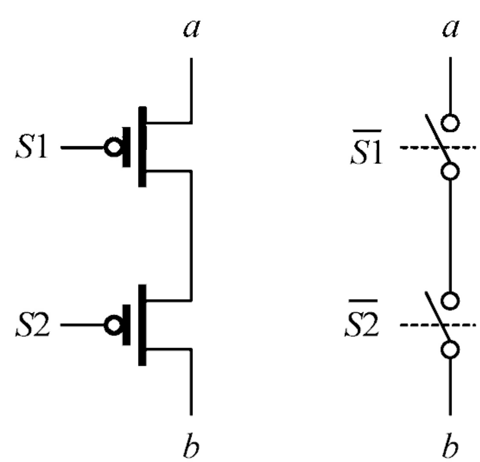
Basic Logic Circuits

(a)



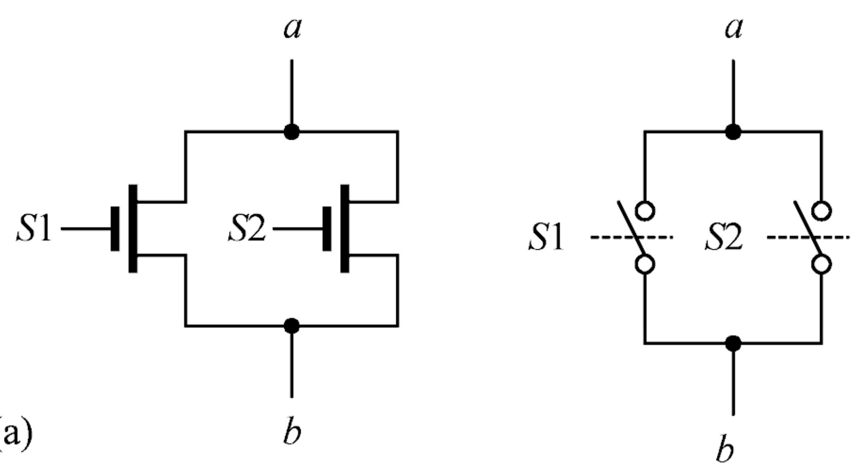
S1 \ S2	0	1
0	off	off
1	off	on

(b)



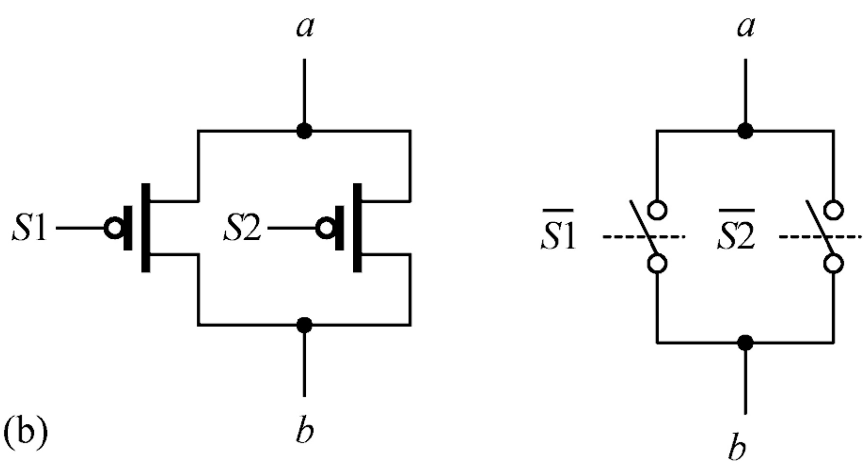
S1 \ S2	0	1
0	on	off
1	off	off

Basic Logic Circuits



S1 \ S2	0	1
0	off	on
1	on	on

(a)

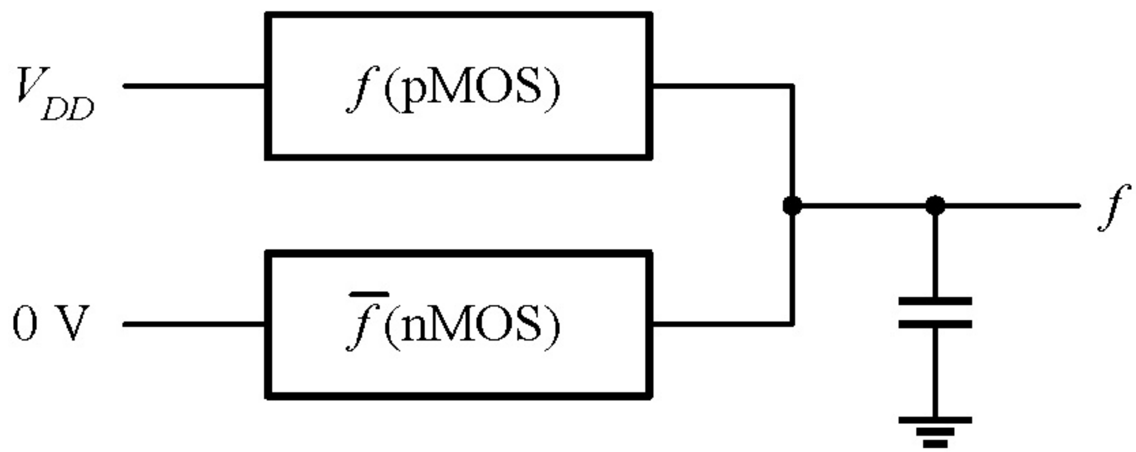


S1 \ S2	0	1
0	on	on
1	on	off

(b)

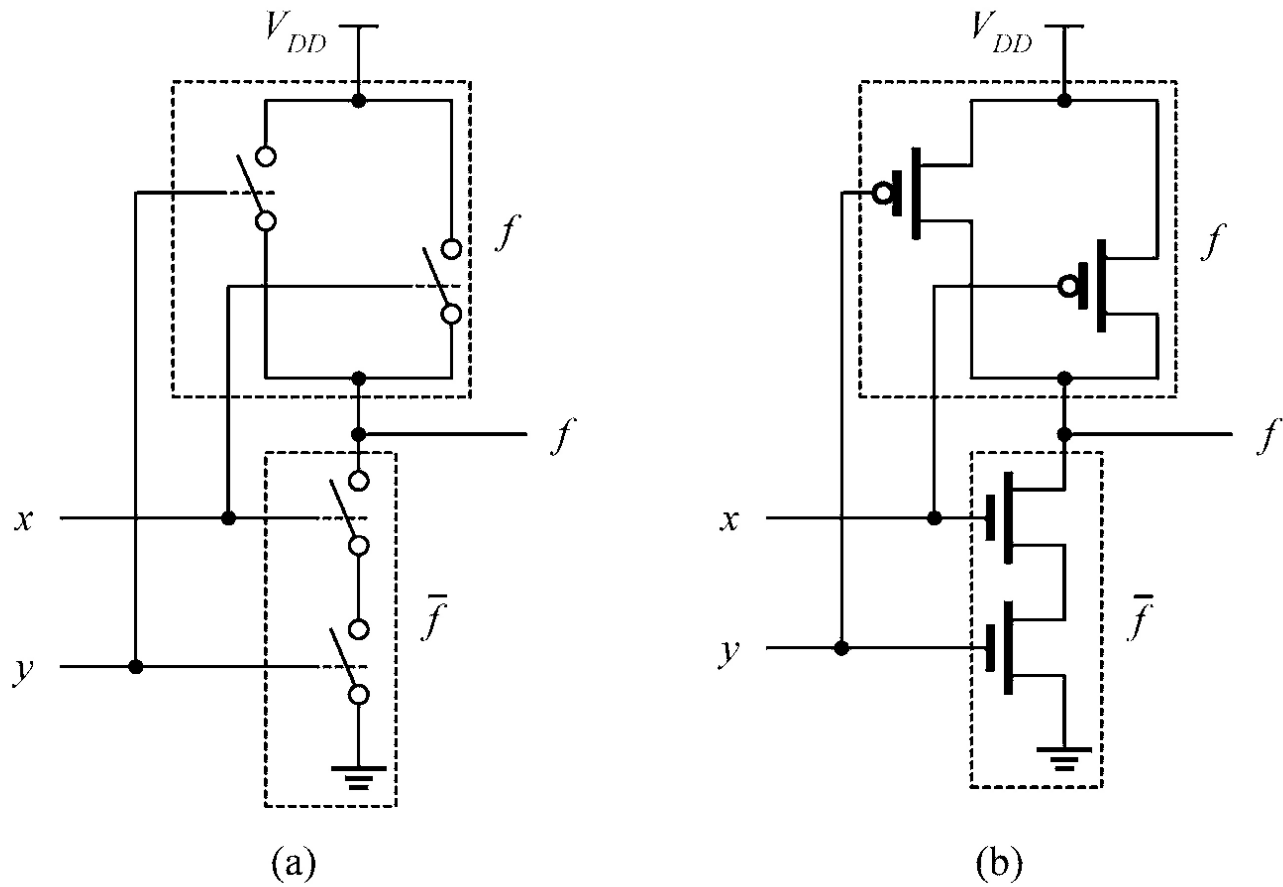
f/*f*' Implementation

- *f*/*f*' implementation (FCMOS)
  - *f* function (pull-up network (PUN)
  - *f*' function (pull-down network (PDN)



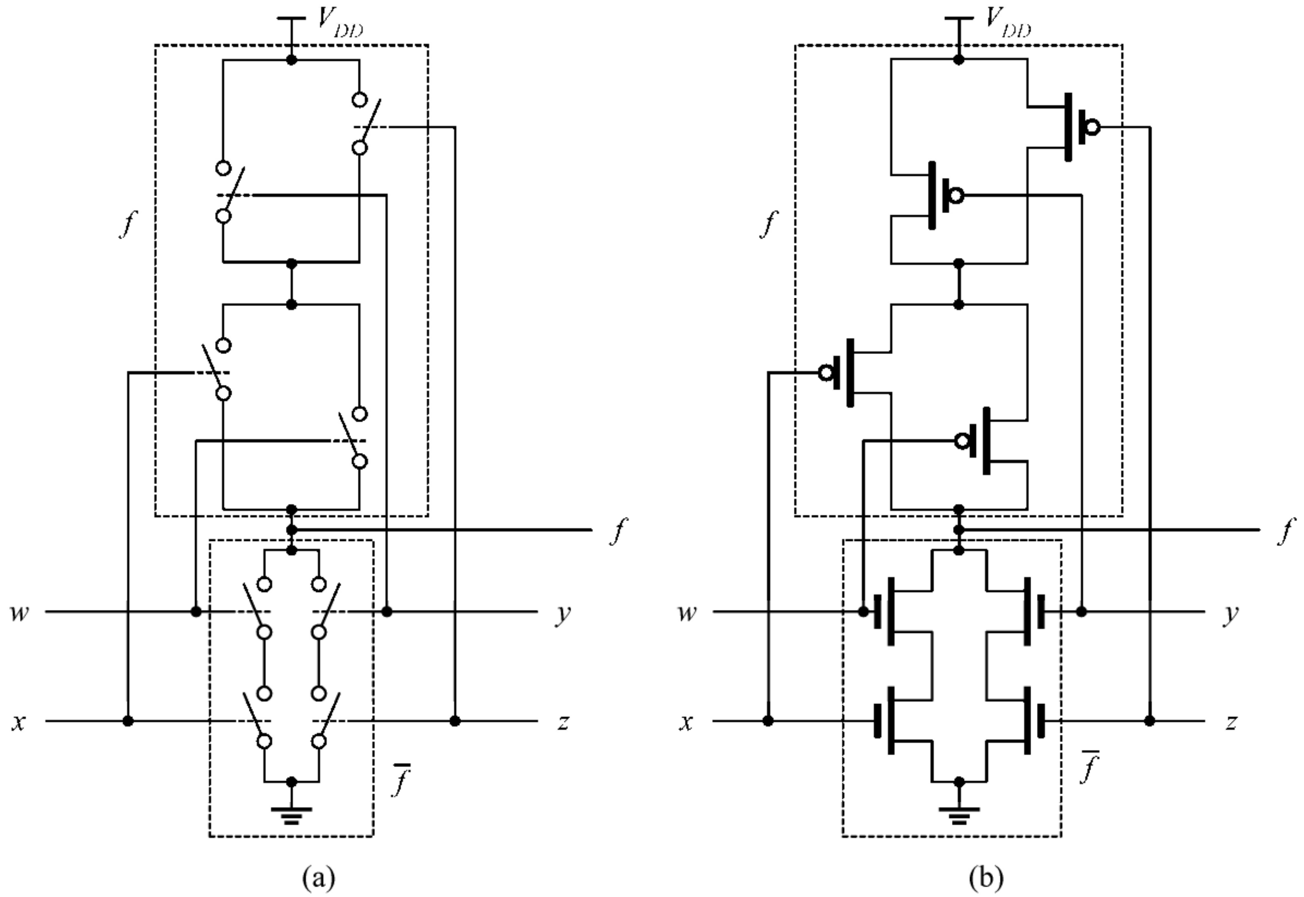
f/f' Implementation

- A two-input NAND gate example



f/f' Implementation

- AND-OR-Inverter (AOI)



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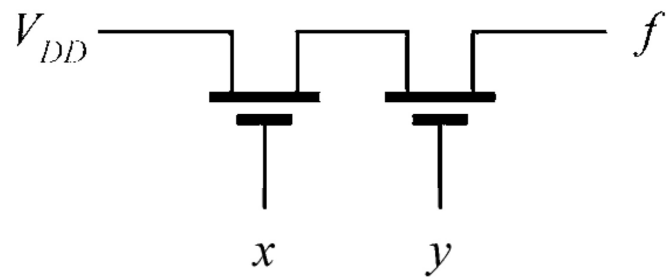
- Basic operations of switches
- Switch logic circuits
  - Switch logic circuits
  - Basic rules
  - Shannon's expansion theorem
  - Residues of a switching function
- Systematic design methodologies

Switch Logic Circuits

- Why the following logic circuit cannot work correctly?

(a)

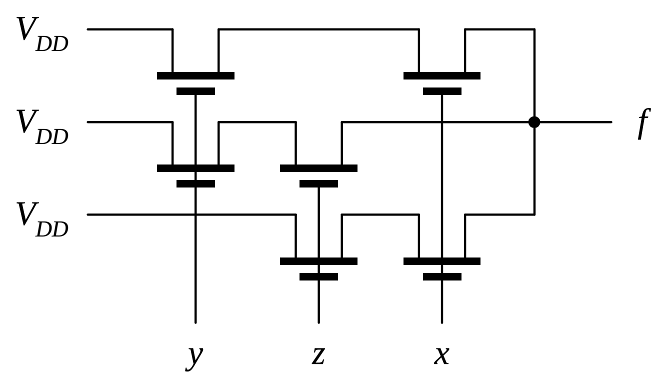


(b)

- Another example

  Can the right logic circuit correctly implement the switching function?

  $f(x, y, z) = xy + yz + yz$



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Basic Rules

- Rule 1 (node-value rule)
  - The function or a signal summing point must always be connected to 0 or 1 at any time
- Rule 2 (node-conflict-free rule)
  - The function or a signal summing point must never be connected to 0 and 1 at the same time

Please always remember these two rules.

Basic Rules

- Rule 1
  - Correct logic function
- Rule 2
  - Distinguishes ratioless logic from ratioed logic
- Ratioless logic
  - Both rules are confined
- What is ratioless logic?

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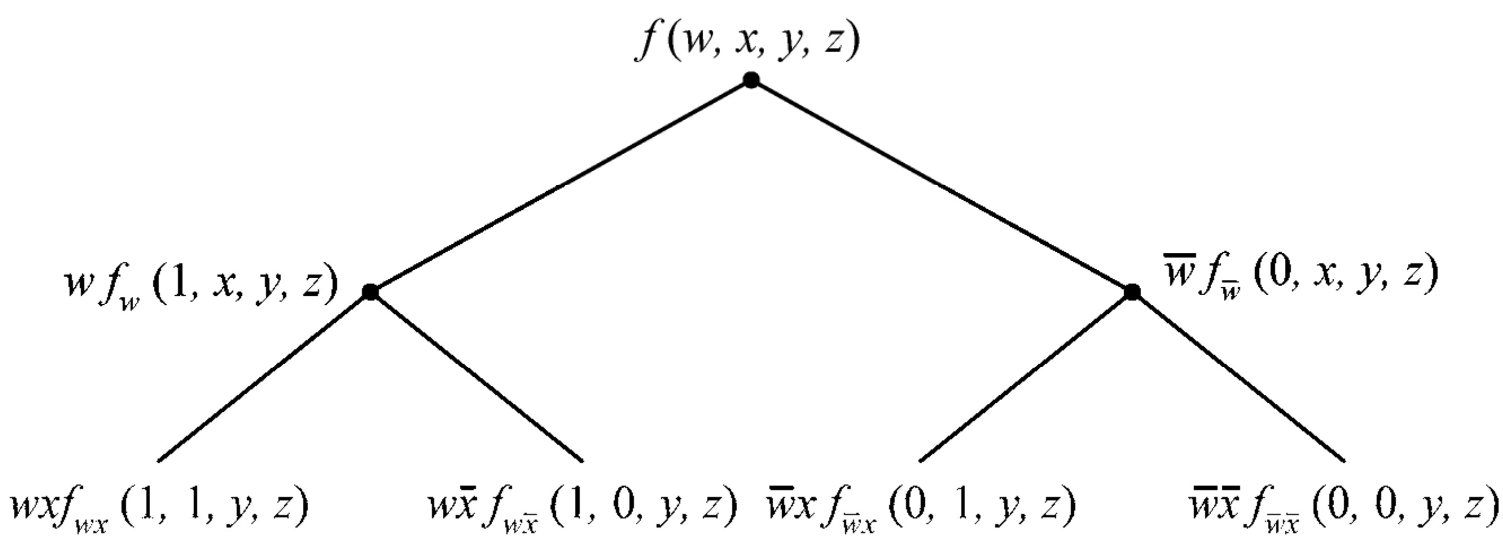
Shannon's Expansion Theorem

- Shannon's expansion theorem

$$f(x_{n-1}, x_{n-2}, \cdots, x_2, x_1, x_0) = x_i f(x_{n-1}, x_{n-2}, \cdots, x_{i+1}, 1, x_{i-1}, \cdots, x_2, x_1, x_0) + \overline{x_i} f(x_{n-1}, x_{n-2}, \cdots, x_{i+1}, 0, x_{i-1}, \cdots, x_2, x_1, x_0)$$

Proof: Trivial.



Shannon's Expansion Theorem

- An example

$$
\begin{aligned}
f(x,y,z) &= xy + xz + yz \\
&= \bar{x} \cdot f(0,y,z) + x \cdot f(1,y,z) \\
&= \bar{x} \cdot (yz) + x \cdot (y + z + yz) \\
&= \bar{x}yz + xy + xz
\end{aligned}
$$

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Residues of a Switching Function

- Let

$$X = \{x_{n-1}, x_{n-2}, \ldots, x_2, x_1, x_0\}$$
$$Y = \{y_{m-1}, y_{n-2}, \ldots, y_2, y_1, y_0\}$$

For all $y_j \in X$

- Residue of $f(X)$ with respect to Y, denote $f_Y(X)$
  - Set all complementary literals equal to 0
  - Set all true literals equal to 1

Residues of a Switching Expression

- Example

$$f(w,x,y,z) = \overline{w}\,\overline{x}y + \overline{w}xy + \overline{w}x\overline{y}z + wxyz + (w\overline{x}y)$$

$$f_{\bar{w}\bar{x}\bar{y}}(0,0,0,z) = 0 \qquad f_{w\bar{x}\bar{y}}(1,0,0,z) = 0$$

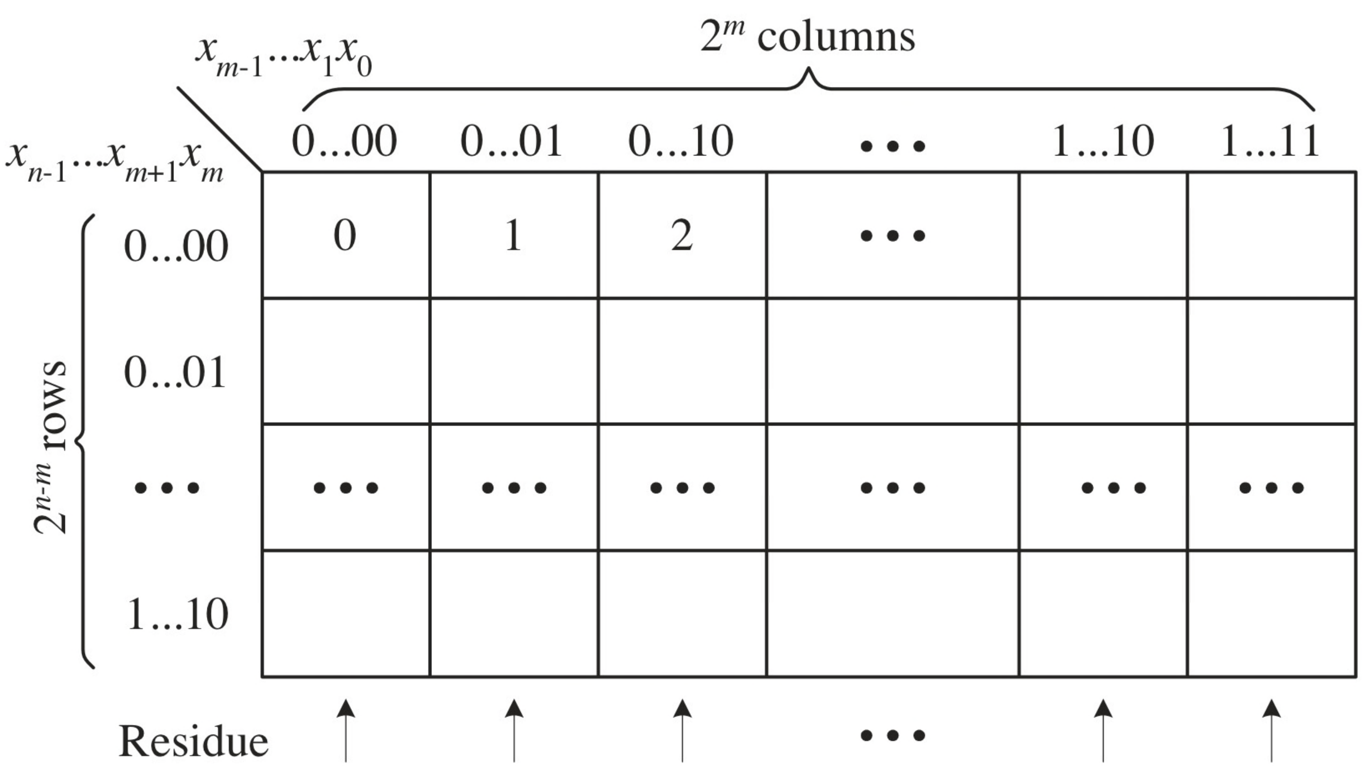
$$f_{\bar{w}\bar{x}y}(0,0,1,z) = 1 \qquad f_{w\bar{x}y}(1,0,1,z) = \phi$$

$$f_{\bar{w}x\bar{y}}(0,1,0,z) = z \qquad f_{wx\bar{y}}(1,1,0,z) = 0$$

$$f_{\bar{w}xy}(0,1,1,z) = 1 \qquad f_{wxy}(1,1,1,z) = z$$

Residue Map --- General Form

- Let $X = \{x_{n-1}, \ldots, x_1, x_0\}$
  $Y = \{y_{m-1}, \ldots, y_1, y_0\}$



Residue Map Example

- $f(w, x, y, z) = \Sigma(0, 1,3, 5, 6, 10, 14)$.

w \ xyz	000	001	010	011	100	101	110	111
0	0	1	2	3	4	5	6	7
1	8	9	10	11	12	13	14	15

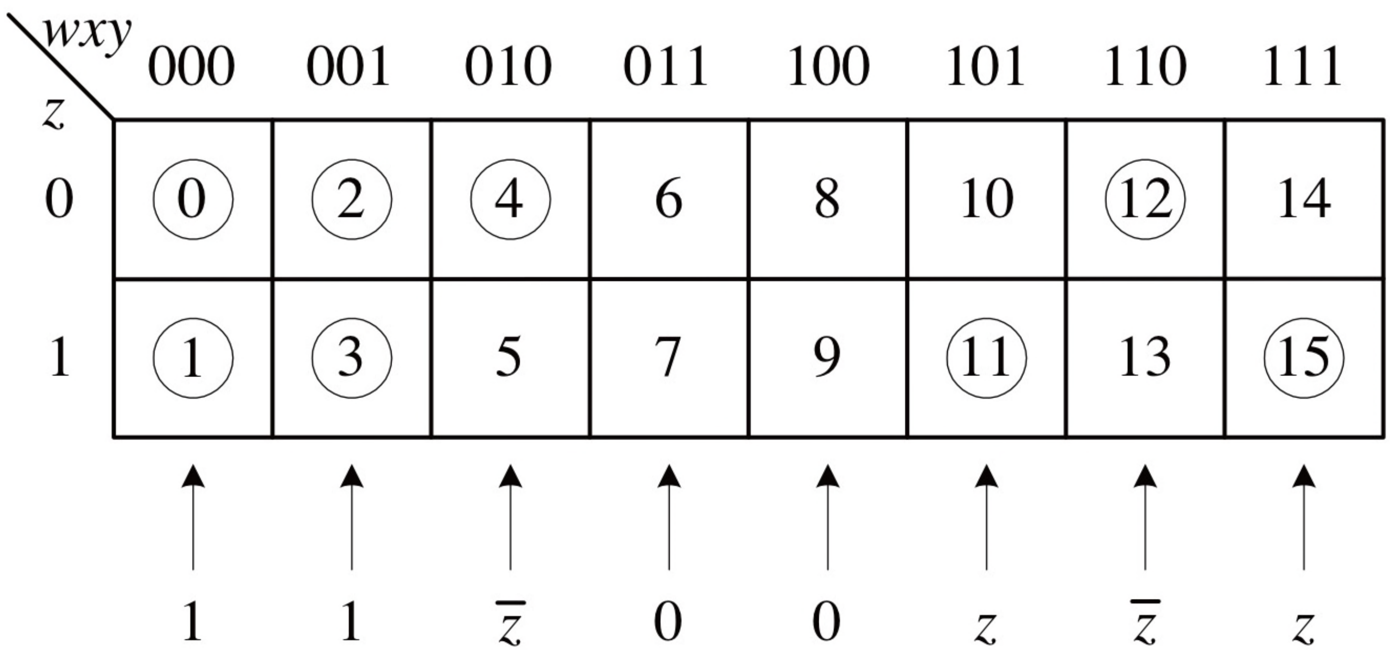
Residue Map Example

- $f(v, w, x, y, z) = \Sigma\,(1, 7, 9, 11, 13, 22, 25, 26, 27, 30, 31) + \Sigma_{\phi}\,(15, 17, 19, 23)$

vw \ xyz	000	001	010	011	100	101	110	111
00	0	1	2	3	4	5	6	7
01	8	9	10	11	12	13	14	15*
11	24	25	26	27	28	29	30	31
10	16	17*	18	19*	20	21	22	23*

Residue Map Example

- $f(w, x, y, z) = \Sigma\,(0, 1, 2, 3, 4, 6, 11, 12, 15)$



Residue Map Example

$vw \backslash xyz$	000	001	010	011	100	101	110	111
00	0	1	2	3	4	5	6*	7
01	8	9	10	11	12	13	14*	15
11	24	25	26	27	28	29	30*	31
10	16	17*	18	19*	20	21	22*	23
	0	1	vw	w	0	$\bar{v}w$	ϕ	0

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- Basic operations of switches
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- Systematic design methodologies
  - Tree network
  - 0/1-x/x’-tree network
  - 0/1-tree network

Systematic Design Methods

- Tree networks
  - Uniform-tree network
  - Freeform-tree network
- 0/1-*x*/*x*'-tree network
- 0/1-tree networks
  - General 0/1-tree network
  - *f*/*f*' paradigm

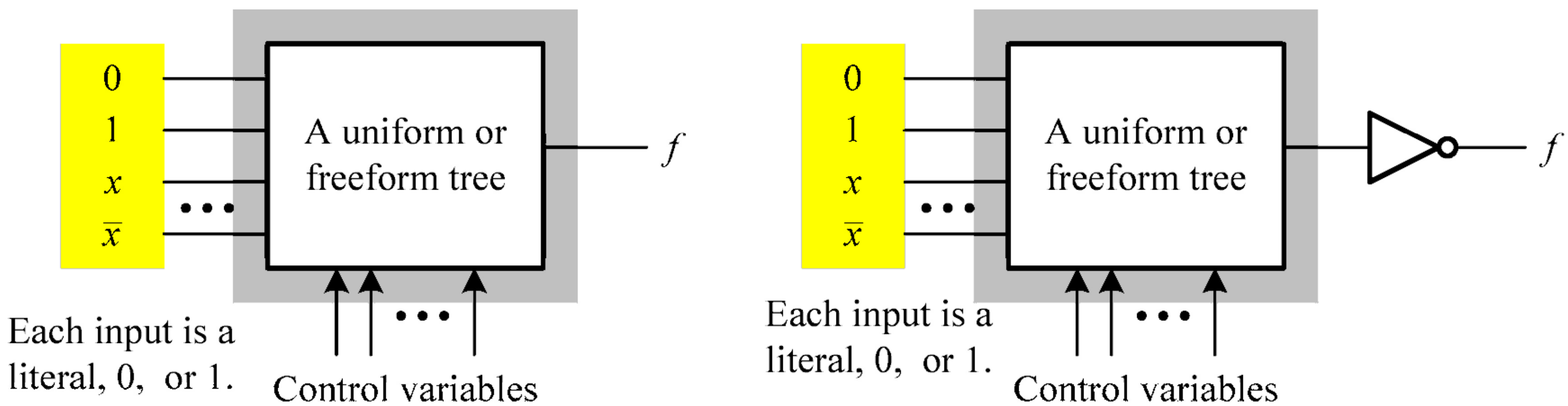
Tree Networks

- Basic design method
  - Repeatedly apply Shannon's expansion theorem
  - Trivial literals (x and x')
- Types of tree networks
  - Freeform-tree network
  - Uniform- tree network

Tree Networks

Implementations

- Using CMOS switches
- Using nNMOS switches



(a) Using CMOS switches (b) Using nMOS switches

Freeform-Tree Network

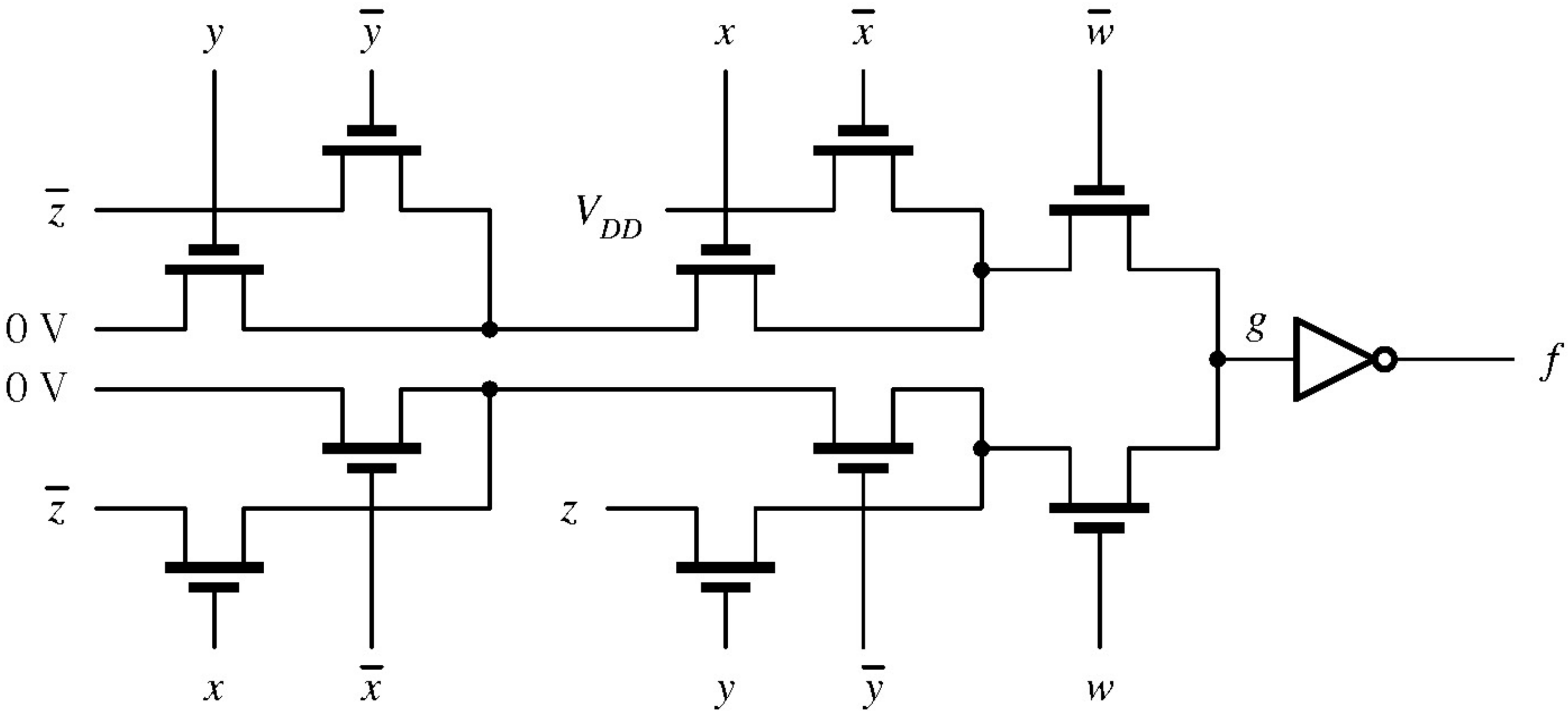
- Example

$$f(w,x,y,z) = \overline{(\bar{w}\bar{x} + x\bar{y}\bar{z} + wyz)}$$

- Let

$$\begin{aligned}
g = \bar{f} &= \bar{w}\bar{x} + x\bar{y}\bar{z} + wyz \\
&= \bar{w}(\bar{x} + x\bar{y}\bar{z}) + w(x\bar{y}\bar{z} + yz) \\
&= \bar{w}[\bar{x}(1) + x(\bar{y}\bar{z})] + w[\bar{y}(x\bar{z}) + y(z)] \\
&= \bar{w}\{\bar{x}(1) + x[\bar{y}(\bar{z}) + y(0)]\} + w\{\bar{y}[\bar{x}(0) + x(\bar{z})] + y(z)\}
\end{aligned}$$

Freeform-Tree Network



Uniform-Tree Network

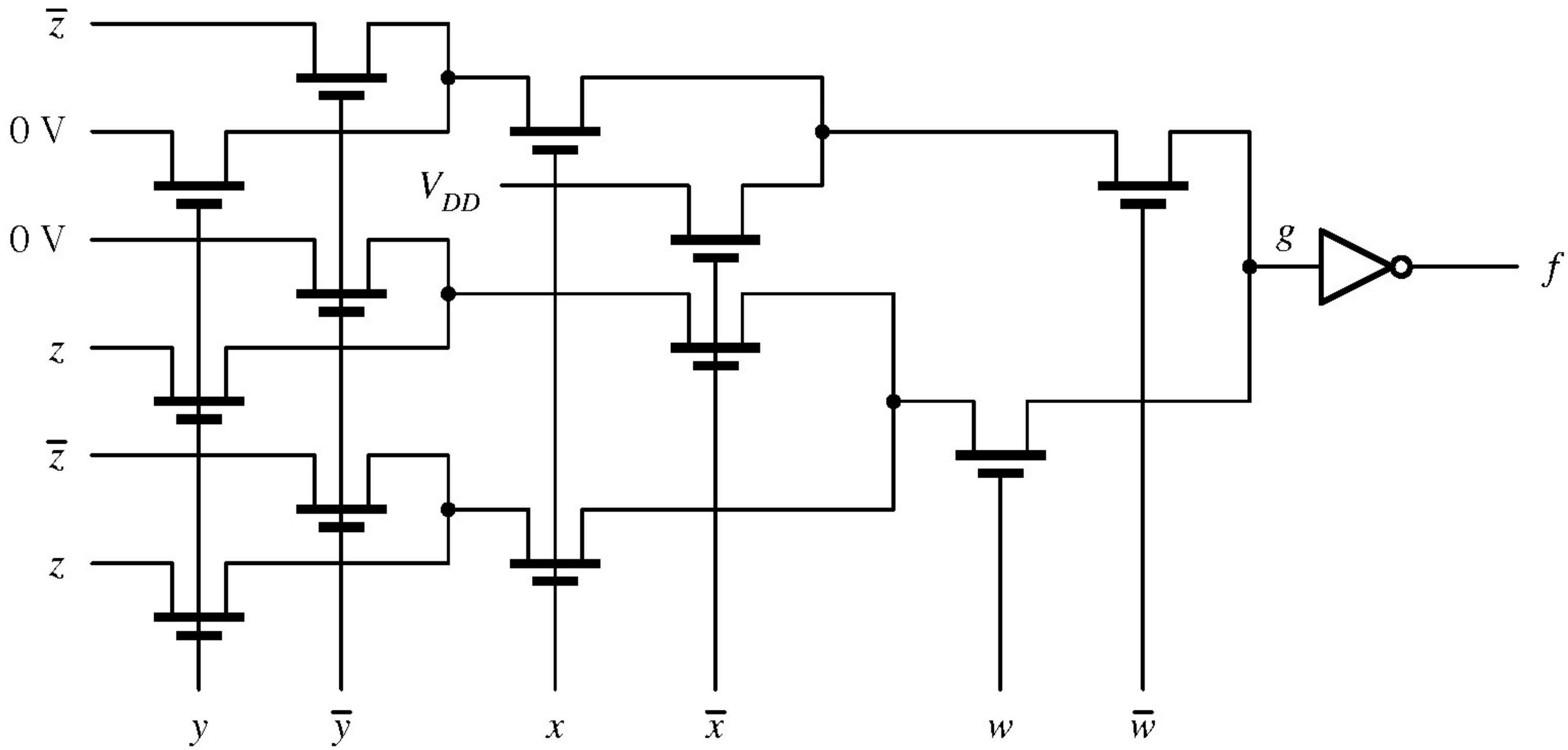
- Example

$$f(w,x,y,z) = \overline{(\bar{w}\bar{x} + x\bar{y}\bar{z} + wyz)}$$

- Let

$$\begin{aligned} g = \bar{f} &= \bar{w}\bar{x} + x\bar{y}\bar{z} + wyz \\ &= \bar{w}(\bar{x} + x\bar{y}\bar{z}) + w(x\bar{y}\bar{z} + yz) \\ &= \bar{w}[\bar{x}(1) + x(\bar{y}\bar{z})] + w[\bar{x}(yz) + x(\bar{y}\bar{z} + yz)] \\ &= \bar{w}\{\bar{x}(1) + x[\bar{y}(\bar{z}) + y(0)]\} + w\{\bar{x}\{[\bar{y}(0) + y(z)] + x[\bar{y}(\bar{z}) + y(z)]\}\} \end{aligned}$$

Uniform-Tree Network



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  - Tree network
  - 0/1-x/x'-tree network
  - 0/1-tree network

0/1-*x*/*x*'-Tree Networks

- 0/1-*x*/*x*′ network
  - Apply Shannon's expansion theorem
  - Literals *x*, *x*′ and/or constants 0/1
- Constraints:

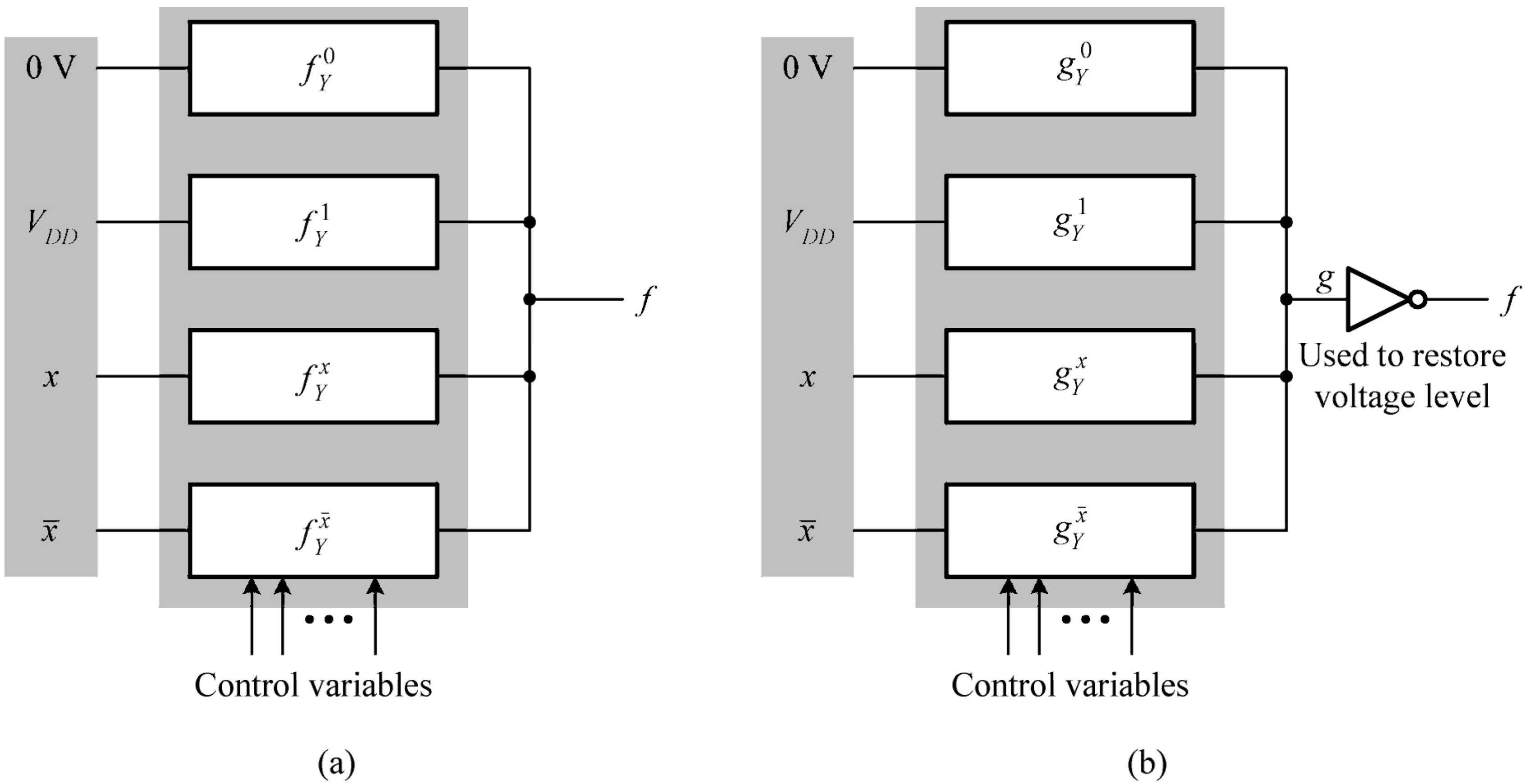
$$f_Y^0 \cup f_Y^1 \cup f_Y^x \cup f_Y^{\bar{x}} = 1$$

$$f_Y^0 \cap f_Y^1 \cap f_Y^x \cap f_Y^{\bar{x}} = \varphi$$

f_Y^s is the set of any combinations of Y such that $R_Y(X) = s$, where $s \in \{0, 1, x, x'\}$

0/1-*x*/*x*'-Tree Networks

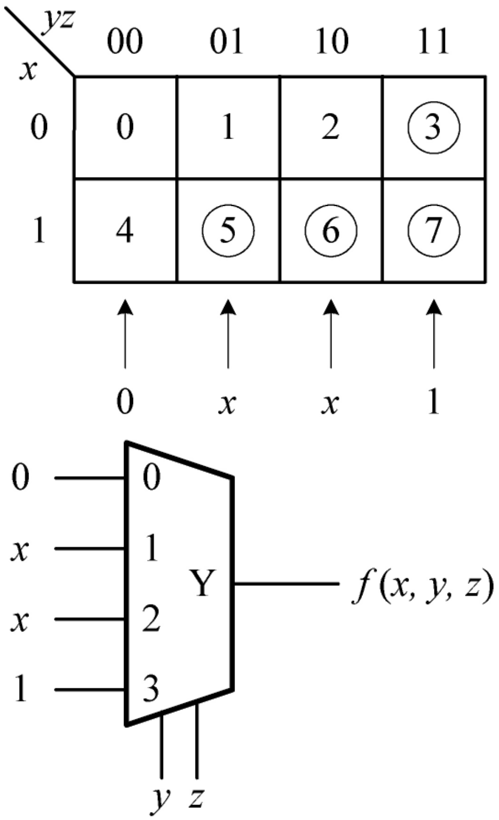
- General paradigms

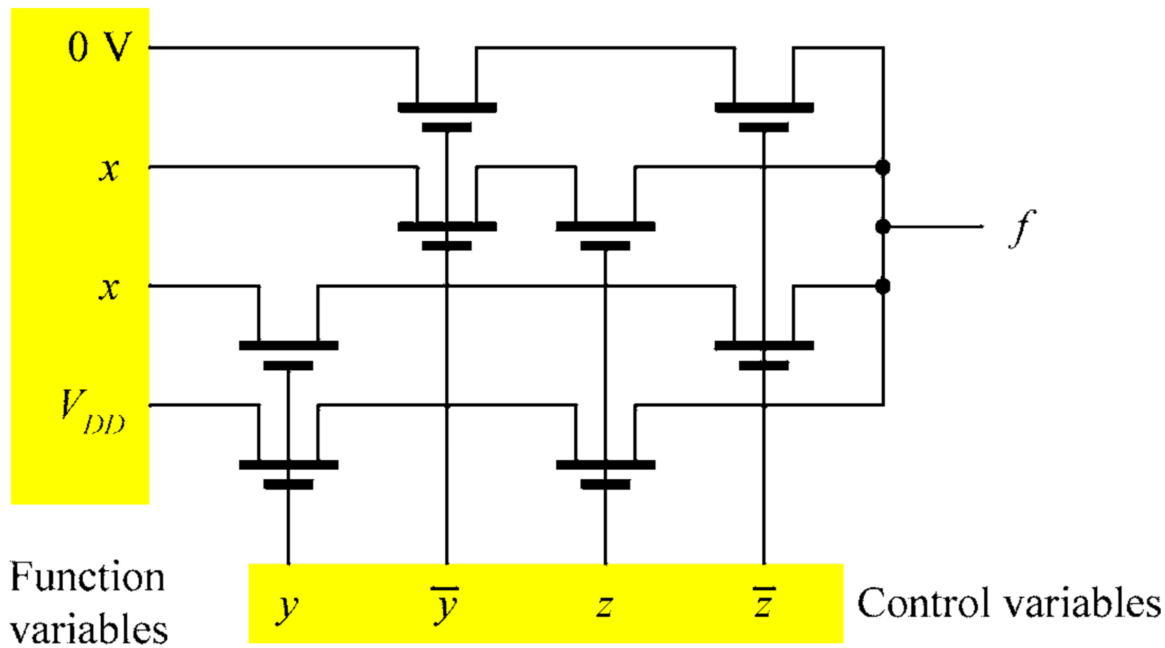


0/1-*x*/*x*'-Tree Network Example

- Realize the following switching function

$$f(x, y, z) = xy + xz + yz$$





0/1-*x*/*x*'-Tree Network Example

- Example

$$f(w,x,y,z) = \overline{(\bar{w}\bar{x} + x\bar{y}\bar{z} + wyz)}$$

$$g = \bar{f}(w,x,y,z) = \bar{w}\bar{x} + x\bar{y}\bar{z} + wyz$$

$$= \sum(0,\ 1,\ 2,\ 3,\ 4,\ 11,\ 12,\ 15)$$

z \ wxy	000	001	010	011	100	101	110	111
0	0	2	4	6	8	10	12	14
1	1	3	5	7	9	11	13	15
	1	1	$\bar{z}$	0	0	z	$\bar{z}$	z

$$f_Y^0 = \bar{w}xy + w\bar{x}\bar{y}$$

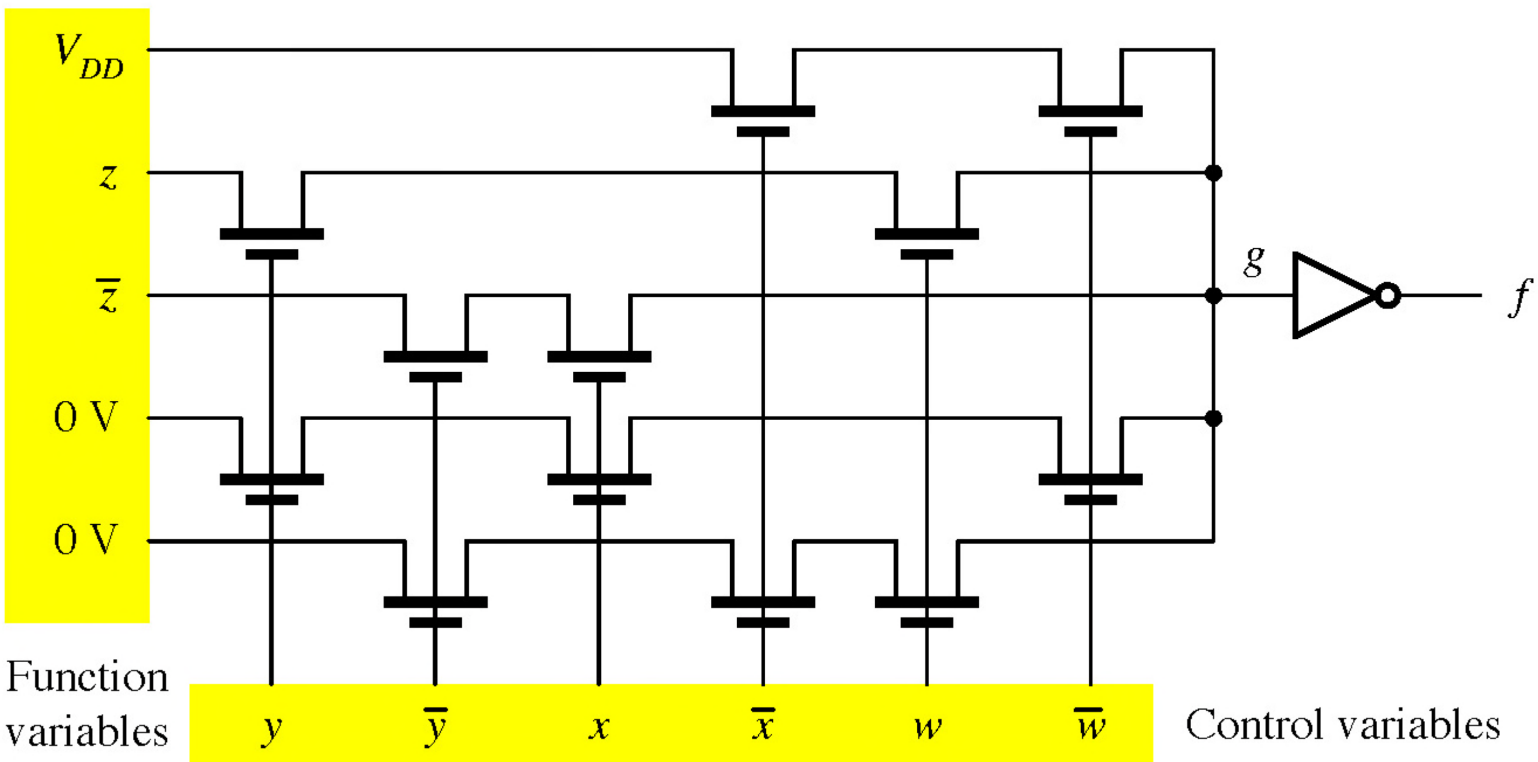
$$f_Y^1 = \bar{w}\bar{x}\bar{y} + \bar{w}\bar{x}y = \bar{w}\bar{x}$$

$$f_Y^z = w\bar{x}y + wxy = wy$$

$$f_Y^{\bar{z}} = \bar{w}x\bar{y} + wx\bar{y} = x\bar{y}$$

0/1-*x*/*x*'-Tree Network Example (continued)

- The resulting logic circuit is as follows:



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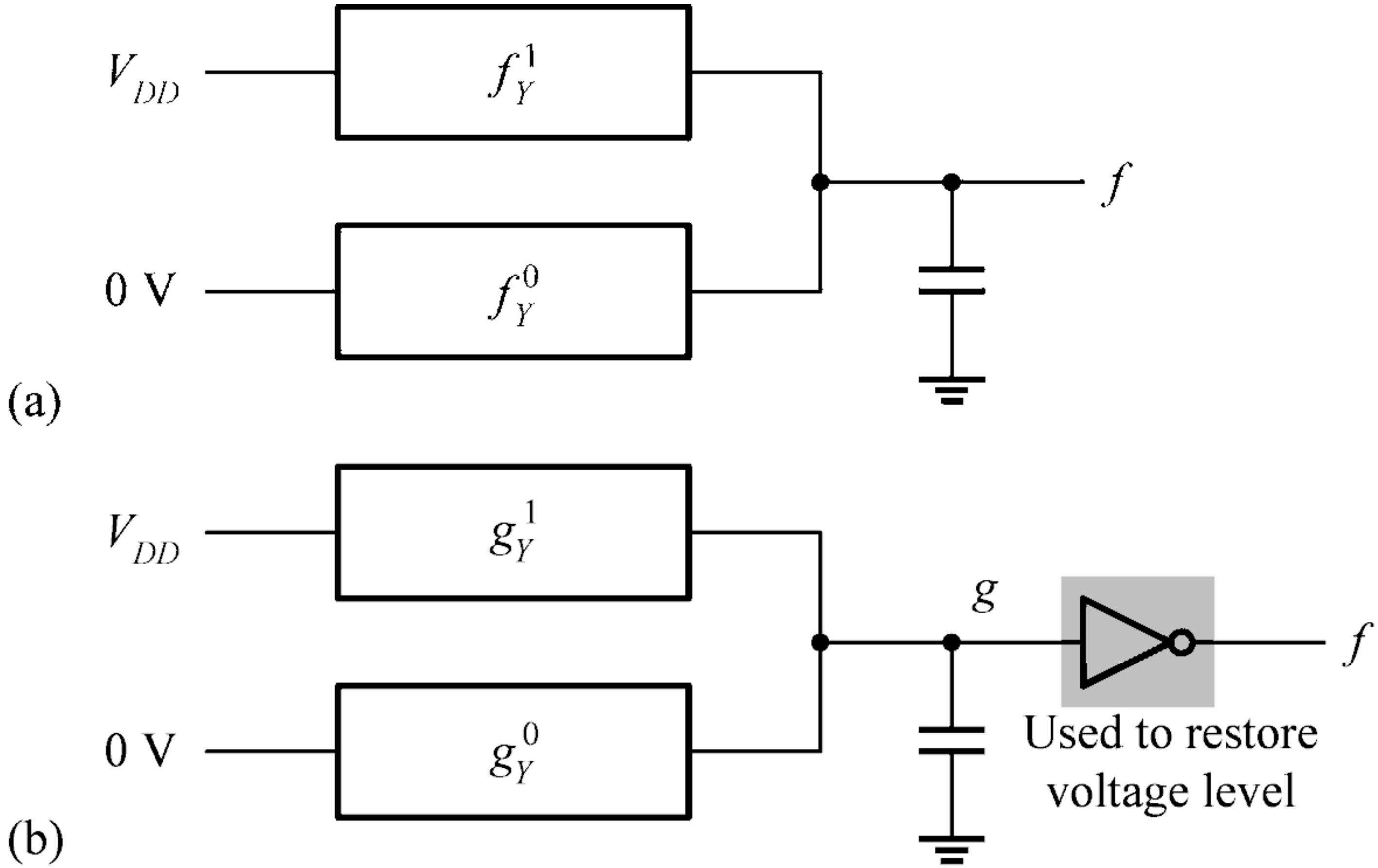
  - 0/1-tree network

0/1-Tree Networks

- General paradigm



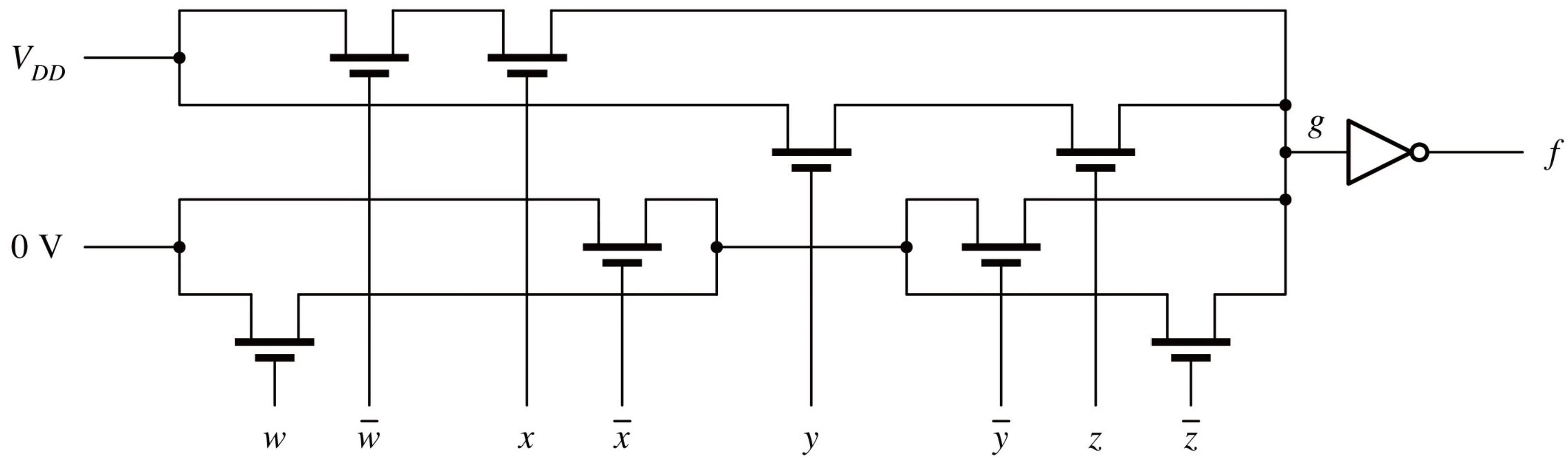
0/1-Tree Network Example

- Example

$$f(w,x,y,z) = \overline{(\overline{w}x + yz)}$$

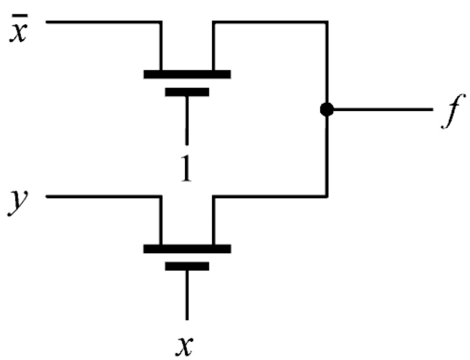
$$g(w,x,y,z) = \overline{f} = \overline{w}x + yz$$

$$\overline{g} = f = \overline{(\overline{w}x + yz)} = (w + \overline{x})(\overline{y} + \overline{z})$$



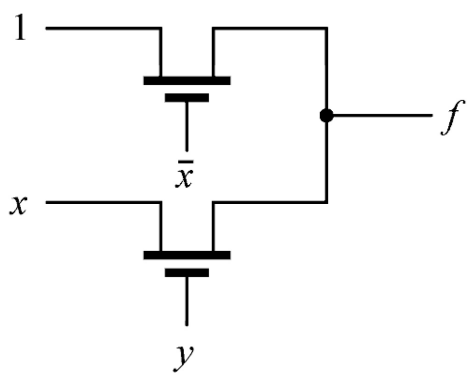
Pitfalls of Shannon's Expansion

$$f(x, y) = \bar{x} + y = \bar{x} \cdot 1 + x \cdot y$$



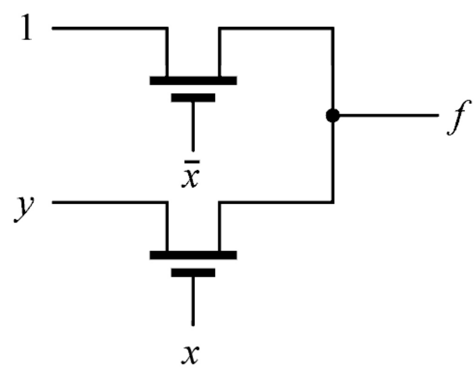
x	y	f
0	0	1
0	1	1
1	0	0
1	1	-

(a)



x	y	f
0	0	1
0	1	-
1	0	-
1	1	1

(b)



x	y	f
0	0	1
0	1	1
1	0	0
1	1	1

(c)