2

Fundamentals of MOS Transistors

Problems

2-1. Calculate the intrinsic carrier concentration of silicon at (a) $T = 350$ K and (b) $T = 650$ K.

Solution: From Equation (2.1)), we obtain the values of bandgap energy E_g at temperature 350 K and 650 K are 1.11 eV and 1.02 eV, respectively. Hence, the intrinsic carrier concentrations of silicon at these two temperatures can be computed using Equation (2.13) and are as follows:

(a) At $T = 300$ K:

$$n_i^2 = 6.2 \times 10^{31} \times 350^3 \exp\left(\frac{-1.11}{350 \times 8.62 \times 10^{-5}}\right) = 2.79 \times 10^{23}$$

Therefore, the intrinsic carrier concentration n_i at temperature 350 K is $5.28 \times 10^{11}/\text{cm}^3$

(b) At $T = 650$ K:

$$n_i^2 = 6.2 \times 10^{31} \times 650^3 \exp\left(\frac{-1.02}{650 \times 8.62 \times 10^{-5}}\right) = 2.11 \times 10^{32}$$

Therefore, the intrinsic carrier concentration n_i at temperate 600 K is $1.45 \times 10^{16}/\text{cm}^3$.

2-2. Consider a p-type silicon doped with boron impurity and assume that the concentration of boron impurity is 8.5×10^{15} cm^{-3}.

(a) Calculate the Fermi potential of the p-type material.

(b) Calculate the thermal-equilibrium electron concentration at $T = 300$ K.

Solution: The Fermi potential and thermal-equilibrium electron concentration are computed separately as follows:

(a) The Fermi potential can be computed by using Equation (2.15):

$$\begin{aligned}\phi_{fp} &= -\frac{kT}{e}\ln\left(\frac{N_a}{n_i}\right) \\ &= -25.86 \times 10^{-3}\ln\left(\frac{8.5 \times 10^{15}}{1.45 \times 10^{10}}\right) = -0.34 \text{ V}\end{aligned}$$

(b) Assume that at room temperature all acceptor atoms are ionized. Hence, $p_0 = N_a$. The thermal-equilibrium electron concentration can then be obtained from the mass-action law:

$$n_0 = \frac{n_i^2}{p_0} = \frac{(1.45 \times 10^{10})^2}{8.5 \times 10^{15}} = 2.47 \times 10^4 \text{ cm}^{-3}$$

2-3. Consider an n-type silicon doped with antimony impurity and assume that at $T = 300$ K. The Fermi energy is 0.35 eV below the conduction band.

(a) Calculate the concentration of antimony impurity, assuming that all impurity atoms are ionized.

(b) Calculate the thermal-equilibrium hole concentration.

Solution: The antimony impurity and thermal-equilibrium hole concentrations are computed separately as follows:

(a) The bandgap energy of silicon at $T = 300$ K is 1.125 eV and $e\phi_{fn}$ is equal to $\frac{E_g}{2} - 0.35 = 0.21$ eV. That is, $\phi_{fn} = 0.21$ V. The concentration of antimony impurity can be computed by using Equation (2.17):

$$0.21 = 25.86 \times 10^{-3} \ln\left(\frac{N_d}{1.45 \times 10^{10}}\right)$$

Solving it, the concentration of antimony impurity is found to be 4.88×10^{13} cm^{-3}.

(b) The thermal-equilibrium hole concentration can be obtained from the mass-action law:

$$p_0 = \frac{n_i^2}{n_0} = \frac{(1.45 \times 10^{10})^2}{4.88 \times 10^{13}} = 4.3 \times 10^6 \text{ cm}^{-3}$$

2-4. Assume that a p-type material with impurity concentration of $N_a = 5 \times 10^{18}/\text{cm}^3$ and an n-type material with impurity concentration of $N_d = 8.4 \times 10^{15}/\text{cm}^3$ are combined into a pn junction. Calculate the built-in potential of the pn junction at $T = 300$ K.

Solution: The built-in potential can be calculated as follows:

$$\begin{aligned}
\phi_0 &= \frac{kT}{e} \ln \frac{N_d N_a}{n_i^2} \\
&= \frac{8.62 \times 10^{-5} (e\text{V/K}) \times 300 \text{ K}}{e} \ln \frac{8.4 \times 10^{15} \times 5 \times 10^{18}}{(1.45 \times 10^{10})^2} \\
&= 1.00 \text{ V}
\end{aligned}$$

2-5. Consider a pn junction with acceptor and donor concentrations of $N_a = 1.2 \times 10^{18}/\text{cm}^3$ and $N_d = 2.6 \times 10^{15}/\text{cm}^3$, respectively. Calculate the width of depletion region at $T = 300$ K.

Solution: Using the fact that $N_a \gg N_d$, we have:

$$\begin{aligned}
x_n &= \sqrt{\frac{2\varepsilon_s \phi_0}{e}\left(\frac{1}{N_d}\right)} \\
&= \sqrt{\frac{2 \times 11.7 \times 8.85 \times 10^{-14} \times 0.78}{1.6 \times 10^{-19}}\left(\frac{1}{2.6 \times 10^{15}}\right)} = 0.623 \ \mu\text{m}
\end{aligned}$$

The built-in potential ϕ_0 is given as follows:

$$\begin{aligned}
\phi_0 &= \frac{8.62 \times 10^{-5} (e\text{V/K}) \times 300 \text{ K}}{e} \ln \frac{1.2 \times 10^{18} \times 2.6 \times 10^{15}}{(1.45 \times 10^{10})^2} \\
&= 0.78 \text{ V}
\end{aligned}$$

2-6. Represent the junction capacitance versus the applied diode voltage V. The diode is formed between the n-well and p-type substrate. The area and depth of the n-well are 80×60 μm^2 and 2 μm, respectively, as shown in Figure 2.8(a). Suppose that $N_a = 4.5 \times 10^{16}$ cm^{-3} and $N_d = 1.6 \times 10^{17}$ cm^{-3}. The measured zero-bias junction capacitance is 85 aF/μm^2 and $m = 0.45$.

Solution: The built-in potential ϕ_0 is calculated as follows:

$$\begin{aligned}\phi_0 &= \frac{8.62\times10^{-5}(\text{eV/K})\times 300\text{ K}}{e}\ln\frac{4.5\times10^{16}\times1.6\times10^{17}}{(1.45\times10^{10})^2}\\ &= 0.81\text{ V}\end{aligned}$$

The zero-bias junction capacitance consists of two parts: bottom capacitance C_{j0b} and sidewall capacitance C_{j0sw}. The bottom capacitance under zero-bias condition can be calculated as follows:

$$\begin{aligned}C_{j0b} &= C_{j0}\times(80\times60\ \mu\text{m}^2)\\ &= 85\text{ aF}/\mu\text{m}^2\times(80\times60\ \mu\text{m}^2)\\ &= 0.41\text{ pF}\end{aligned}$$

The sidewall capacitance under zero-bias condition can be calculated as in the following:

$$\begin{aligned}C_{j0sw} &= C_{j0}\times(280\times2\ \mu\text{m}^2)\\ &= 85\text{ aF}/\mu\text{m}^2\times(280\times2\ \mu\text{m}^2)\\ &= 0.048\text{ pF}\end{aligned}$$

Therefore, the total zero-bias junction capacitance is 0.46 pF. Using Equation (2.51), the junction capacitance can then be expressed as:

$$C_j = 0.46\left[1-\frac{V}{0.81}\right]^{-0.45}\quad(\text{pF})$$

2-7. For an abrupt n^+p junction diode with $N_d = 4.5\times10^{18}$ cm^{-3} and $N_a = 5.6\times10^{15}$ cm^{-3}, assume that the junction area is 50×50 μm^2.

(a) Find ϕ_0 and C_{j0} at $T = 300$ K.

(b) Find C_j for $V = -1.8$ V.

(c) Find C_{eq} for $V_1 = -1.8$ V and $V_2 = 0$ V.

Solution: (a) The built-in potential at zero bias, ϕ_0, can be calculated as follows:

$$\phi_0 = V_t\ln\left(\frac{N_aN_d}{n_i^2}\right) = 0.026\ln\left(\frac{4.5\times10^{18}\times5.6\times10^{15}}{(1.45\times10^{10})^2}\right) = 0.84\text{ V}$$

The zero-bias junction capacitance, C_{j0}, is found to be:

$$\begin{aligned}C_{j0} &= A\left(\frac{e\varepsilon_{si}}{2\phi_0}\frac{N_aN_d}{N_a+N_d}\right)^{1/2}\\ &= 25\times10^{-6}\left(\frac{1.6\times10^{-19}\times11.7\times8.854\times10^{-14}}{2\times0.84}\frac{4.5\times10^{18}\times5.6\times10^{15}}{4.5\times10^{18}+5.6\times10^{15}}\right)^{1/2}\\ &= 0.59\text{ pF}\end{aligned}$$

(b) The junction capacitance C_j at $V = -1.8$ V is:

$$C_j = \frac{C_{j0}}{[1-(V/\phi_0)]^m} = \frac{0.59\text{ pF}}{[1-(-1.8/0.84)]^{0.5}} = 0.33\text{ pF}$$

(c) The equivalent capacitance C_{eq} for the two extreme voltage values, $V_1 = -1.8$ V and $V_2 = 0$ V, is as follows:

$$\begin{aligned} C_{eq} &= -\frac{C_{j0}\phi_0}{(V_2 - V_1)(1-m)}\left[\left(1-\frac{V_2}{\phi_0}\right)^{1-m} - \left(1-\frac{V_1}{\phi_0}\right)^{1-m}\right] \\ &= -\frac{0.59 \times 0.84}{(0+1.8)(1-0.5)}\left[\left(1-\frac{0}{0.84}\right)^{0.5} - \left(1+\frac{1.8}{0.84}\right)^{0.5}\right] \\ &= 0.43 \text{ pF} \end{aligned}$$

2-8. Supposing that the p-type substrate has impurity concentration of $N_a = 6.5 \times 10^{15}$ cm^{-3} and using $n_i = 1.45 \times 10^{10}$ cm^{-3}, find the maximum depletion layer thickness $x_{d(max)}$ at $T = 300$ K.

Solution: From Equation (2.8), we obtain

$$|\phi_{fp}| = V_t \ln\left(\frac{N_a}{n_i}\right) = 0.026 \ln\left(\frac{6.5 \times 10^{15}}{1.45 \times 10^{10}}\right) = 0.34 \text{ V}$$

The maximum depletion layer thickness is:

$$\begin{aligned} x_{d(max)} &= \sqrt{\frac{4\varepsilon_{si}|\phi_{fp}|}{eN_a}} = \sqrt{\frac{4 \times 11.7 \times 8.854 \times 10^{-14} \times 0.34}{1.6 \times 10^{-19} \times 6.5 \times 10^{15}}} \\ &= 0.37 \ \mu\text{m} \end{aligned}$$

2-9. Assume that the substrate is n-type with donor concentration of $N_d = 2 \times 10^{16}$ cm^{-3} and the temperature is 300 K. ϕ_G and ϕ_{Si} are the work function (Fermi energy level) of gate and silicon substrate, respectively. Referring to Figure 2.1, complete Table 2.10 if electron affinity is 4.05 eV and bandgap energy $E_g = 1.12$ eV.

Table 2.10: The Table for Problem **2-9**

	Aluminum	p^+ polysilicon	n^+ polysilicon
ϕ_G (V)	4.10	5.17	4.05
ϕ_{Si} (V)			
V_{FB} (V)			

Solution: The Fermi potential of the n-type substrate is equal to

$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right) = 0.026 \ln\left(\frac{2 \times 10^{16}}{1.45 \times 10^{10}}\right) = 0.37 \text{ V}$$

Hence, the ϕ_{Si} of the n-type substrate is equal to:

$$\phi_{Si} = \chi + \frac{E_g}{2e} - \phi_{fn} = 4.05 + 0.56 - 0.37 = 4.24 \text{ V}$$

The flat-band voltages can then be calculated accordingly. The results are listed in STable 2.1.

2-10. For an aluminum-gate MOS system, the gate-oxide thickness t_{ox} is 6.5 nm and $\phi_{GS} = -0.88$ V. Assume that acceptor concentration N_a is 6.5×10^{15} cm^{-3} and Q_{ss} is 6.5×10^{10} cm^{-2}.

(a) Find the threshold voltage V_{Tn} at $T = 300$ K.

STable 2.1: The resulting table of Problem **2-9**.

	Aluminum	p^+ polysilicon	n^+ polysilicon
ϕ_G (V)	4.10	5.17	4.05
ϕ_{Si} (V)	4.24	4.24	4.24
V_{GS} (V)	-0.14	0.93	-0.19

(b) Assuming that delta function is used, find the impurity density required to adjust the threshold voltage to 0.55 V.

Solution:

(a) At $T = 300$ K, the intrinsic carrier concentration n_i is 1.45×10^{10} cm^{-3}. From problem **2-8**, we have $x_{d(max)} = 0.37$ μm. Hence, $Q_{d(max)}$ can be calculated as follows:

$$\begin{aligned} Q_{d(max)} &= eN_a x_{d(max)} \\ &= 1.6 \times 10^{-19} \times 6.5 \times 10^{15} \times 0.37 \times 10^{-4} \\ &= 3.85 \times 10^{-8} \text{ C/cm}^2 \end{aligned}$$

The capacitance C_{ox} of the underlying MOS system is found as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{6.5 \times 10^{-7}} = 5.31 \times 10^{-7} \text{ F/cm}^2$$

The threshold voltage V_{Tn} can then be obtained as follows:

$$\begin{aligned} V_{Tn} &= 2|\phi_{fp}| + Q_{d(max)}\frac{t_{ox}}{\varepsilon_{ox}} + \left(\phi_{GS} - Q_{ss}\frac{t_{ox}}{\varepsilon_{ox}}\right) \\ &= 2 \times 0.34 + \frac{3.85 \times 10^{-8}}{5.31 \times 10^{-7}} - 0.88 - \frac{6.5 \times 10^{10} \times (1.6 \times 10^{-19})}{5.31 \times 10^{-7}} \\ &= -0.15 \text{ V} \end{aligned}$$

(b) In order to adjust the threshold voltage to the desired value of 0.55 V, the required impurity density of ion implementation can be found from Equation (2.38).

$$\Delta V_T = 0.45 - (-0.15) = 0.70 \text{ V} = \frac{eD_I}{C_{ox}}$$

Consequently, the required impurity density of ion implementation is:

$$D_I = \frac{C_{ox}}{e} \times \Delta V_T = \frac{5.31 \times 10^{-7}}{1.6 \times 10^{-19}} \times 0.70 = 2.32 \times 10^{12} \text{ cm}^{-2}$$

2-11. Assume that the gate-oxide thickness t_{ox} is 6.5 nm and $\phi_{GS} = -0.88$ V. The impurity concentration of substrate is $N_a = 6.5 \times 10^{15}$ cm^{-3}. If the body bias V_{SB} is 1.8 V, find the body-effect coefficient γ and the threshold voltage V_{Tn} under this body bias, assuming that the threshold voltage without body bias V_{T0n} is 0.55 V.

Solution: From Problem 2.10, we obtain $C_{ox} = 5.31 \times 10^{-7}$ F/cm^2. The body-effect coefficient γ can be calculated as follows:

$$\begin{aligned} \gamma &= \frac{\sqrt{2\varepsilon_{si} e N_a}}{C_{ox}} \\ &= \frac{\sqrt{2 \times 11.7 \times 8.854 \times 10^{-14} \times 1.6 \times 10^{-19} \times 6.5 \times 10^{15}}}{5.31 \times 10^{-7}} \\ &= 0.09 \ \ (\text{V}^{0.5}) \end{aligned}$$

The threshold voltage with $V_{SB} = 1.8$ V is then calculated as follows:

$$\begin{aligned} V_{Tn} &= V_{T0n} + \gamma\left(\sqrt{2|\phi_{fp}| + V_{SB})} - \sqrt{2|\phi_{fp}|}\right) \\ &= 0.55 + 0.09\left(\sqrt{2\times 0.34 + 1.8} - \sqrt{2\times 0.34}\right) \\ &= 0.62 \text{ V} \end{aligned}$$

where $|\phi_{fp}| = 0.34$ V, from Problem **2-8**.

2-12. Assume that $t_{ox} = 3.2$ nm in a 0.13 μm process.

(a) Calculate the effective electron mobility as $V_{GS} = 1.2$ V and $V_{Tn} = 0.35$ V.

(b) Calculate the effective hole mobility as $V_{GS} = 1.2$ V and $V_{Tp} = -0.35$ V.

Solution: The effective electron and hole mobilities are calculated as follows:

(a) Using Equation (2.87), we have $E_{norm} = 8.07\times 10^5$ V/cm and using Equation (2.86) the effective electron mobility is calculated as $\mu_{eff} = 301$ cm^2/V-s.

(b) Using Equation (2.87), we have $E_{norm} = 4.43\times 10^5$ V/cm and using Equation (2.86) the effective hole mobility is calculated as $\mu_{eff} = 98$ cm^2/V-s.

2-13. Using the parameters given in Table 2.11 and assuming that $2\phi_f = -0.8$ V, determine the device parameters, V_{T0}, k, γ, and λ.

Table 2.11: Parameters for Problem 2.13.

V_{GS}(V)	V_{DS}(V)	V_{SB}(V)	$I_D(\mu$A)
0.8	0.8	0	37
0.8	1.2	0	40
1.2	1.2	0	130
1.2	1.2	0.3	44
1.8	1.8	0.3	178

Solution: Solution: Since the transistor operates in saturation region, the drain current is as follows:

$$I_D(sat) = \frac{1}{2}k_n(V_{GS} - V_{T0n})^2(1 + \lambda V_{DS})$$

(a) Find V_{T0}. From row 3 and row 2, we obtain

$$\frac{I_{dsat}(row\ 3)}{I_{dsat}(row\ 2)} = \frac{(1.2 - V_{T0})^2}{(0.8 - V_{T0})^2} = \frac{130}{40} \tag{2.1}$$

Hence, $V_{T0} = 0.30$ V.

(b) Find λ. From row 3 and row 1, we obtain

$$\frac{I_{dsat}(row\ 3)}{I_{dsat}(row\ 1)} = \frac{(V_{GS} - V_{T0})^2(1 + \lambda V_{DS}(row\ 3))}{(V_{GS} - V_{T0})^2(1 + \lambda V_{DS}(row\ 1))} = \frac{0.81(1 + 1.2\lambda)}{0.25(1 + 0.8\lambda)} = \frac{130}{37} \tag{2.2}$$

Hence, $\lambda = 0.25$ V.

(c) Find k. From row 3, we obtain

$$130 = \frac{1}{2}k(1.2 - 0.30)^2(1 + 0.25\times 1.2)$$

Hence, $k = 247$ μA/V^2.

(d) Find γ. From row 4, we obtain

$$44 = \frac{1}{2}247(1.2 - V_{Tn})^2(1 + 0.25 \times 1.2)$$

Hence, $V_{Tn} = 0.68$ V.

$$0.68 = 0.30 + \gamma(\sqrt{0.8 + 0.3} - \sqrt{0.8})$$

Hence, $\gamma = 2.38$ V.

2-14. Using the parameters given in Table 2.12 and assuming that $2\phi_f = -0.8$ V, determine the device parameters, V_{T0}, k, γ, and λ.

Table 2.12: Parameters for Problem 2.14.

V_{GS}(V)	V_{DS}(V)	V_{SB}(V)	$I_D(\mu$A)
0.8	1.2	0	32
1.2	1.2	0	116
1.2	1.2	0.4	17
1.2	1.8	0	120

Solution: Since the transistor operates in saturation region, the drain current is as follows:

$$I_D(sat) = \frac{1}{2}k_n(V_{GS} - V_{T0n})^2(1 + \lambda V_{DS})$$

(a) Find V_{T0}. From row 2 and row 1, we obtain

$$\frac{I_{dsat}(row\ 2)}{I_{dsat}(row\ 1)} = \frac{(1.2 - V_{T0})^2}{(0.8 - V_{T0})^2} = \frac{116}{32} \tag{2.3}$$

Hence, $V_{T0} = 0.33$ V.

(b) Find λ. From row 4 and row 2, we obtain

$$\frac{I_{dsat}(row\ 4)}{I_{dsat}(row\ 2)} = \frac{1 + \lambda V_{DS}(row\ 4)}{1 + \lambda V_{DS}(row\ 2)} = \frac{1 + 1.8\lambda}{1 + 1.2\lambda} = \frac{120}{116} \tag{2.4}$$

Hence, $\lambda = 0.06$ V.

(c) Find k. From row 2, we obtain

$$116 = \frac{1}{2}k(1.2 - 0.33)^2(1 + 0.06 \times 1.2)$$

Hence, $k = 286\ \mu$A/V^2.

(d) Find γ. From row 3, we obtain

$$17 = \frac{1}{2}286(1.2 - V_{Tn})^2(1 + 0.06 \times 1.2)$$

Hence, $V_{Tn} = 0.87$ V.

$$0.87 = 0.33 + \gamma(\sqrt{0.8 + 0.4} - \sqrt{0.8})$$

Hence, $\gamma = 2.57$ V.

2-15. Show that the temperature dependence of threshold voltage can be expressed as follows:

$$\frac{dV_{Tn}}{dT} = -\frac{1}{T}\left(\frac{E_g}{2e} - |\phi_{fp}|\right)\left(2 + \frac{\gamma}{\sqrt{2|\phi_{fp}|}}\right)$$

Solution: The threshold voltage V_{Tn} can be rewritten as follows:

$$\begin{aligned} V_{Tn} &= 2|\phi_{fp}| + \frac{Q_{d(max)}}{C_{ox}} + V_{FB} \\ &= 2|\phi_{fp}| + \frac{\sqrt{4e\varepsilon_{si}N_a|\phi_{fp}|}}{C_{ox}} + V_{FB} \end{aligned}$$

The dependence of V_{Tn} with temperature can be seen by taking the derivative of V_{Tn} with respect to temperature T:

$$\begin{aligned} \frac{dV_{Tn}}{dT} &= 2\frac{d|\phi_{fp}|}{dT} + \frac{\sqrt{4e\varepsilon_{si}N_a}}{2C_{ox}\sqrt{|\phi_{fp}|}}\frac{d|\phi_{fp}|}{dT} \\ &= \frac{d|\phi_{fp}|}{dT}\left[2 + \frac{\gamma}{\sqrt{2|\phi_{fp}|}}\right] \end{aligned}$$

where $|\phi_{fp}|$ is also a function of temperature and can be further expressed as follows:

$$\begin{aligned} |\phi_{fp}| &= \frac{kT}{e}\ln\left(\frac{N_a}{n_i}\right) \\ &= \frac{kT}{e}\ln\left(\frac{N_a \exp\left(\frac{E_g}{2kT}\right)}{\sqrt{N_v N_c}}\right) \end{aligned}$$

In the second equation, we substitute the n_i with the following expression:

$$n_i = \sqrt{N_v N_c}\exp\left(-\frac{E_g}{2kT}\right)$$

where we use the fact that $n_i^2 = n_0 p_0$. Consequently, the dependence of $|\phi_{fp}|$ with temperature can be expressed as:

$$\begin{aligned} \frac{d|\phi_{fp}|}{dT} &= \frac{kT}{e}\left(-\frac{E_g}{2kT^2}\right) + \frac{k}{e}\ln\left(\frac{N_a \exp\left(\frac{E_g}{2kT}\right)}{\sqrt{N_v N_c}}\right) \\ &= -\frac{1}{T}\left(\frac{E_g}{2e} - |\phi_{fp}|\right) \end{aligned}$$

Therefore,

$$\frac{dV_{Tn}}{dT} = -\frac{1}{T}\left(\frac{E_g}{2e} - |\phi_{fp}|\right)\left(2 + \frac{\gamma}{\sqrt{2|\phi_{fp}|}}\right)$$

2-16. The well-defined temperature dependence of diode voltage can be used to develop a voltage that is directly proportional to absolute temperature (PTAT). This voltage is referred as the PTAT voltage or V_{PTAT}.

(a) Referring to Figure 2.34, show that

$$V_{PTAT} = V_t \ln\left(\frac{I_{D1}}{I_{D2}}\right)$$

(b) Calculate V_{PTAT} if I_1 is set to 10 times I_2.

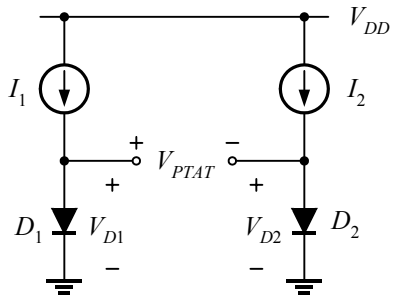

Figure 2.34: The circuit of PTAT.

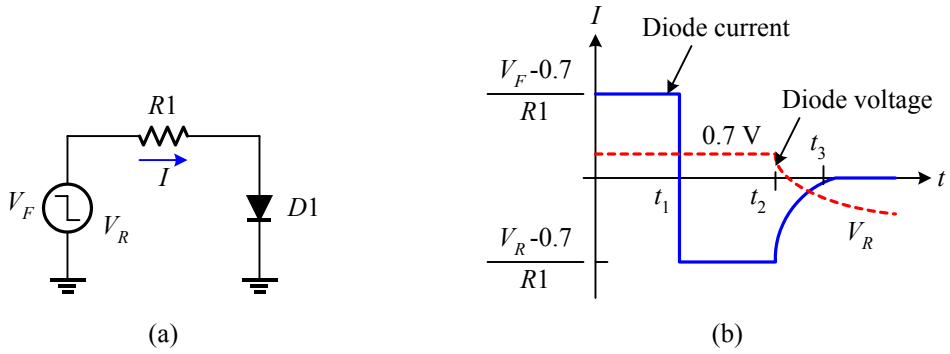

Figure 2.35: The (a) circuit of a *pn*-junction diode for studying (b) transition characteristic.

Solution:

(a) From Figure 2.34, we obtain

$$\begin{aligned} V_{PTAT} &= V_{D1} - V_{D2} = V_t \ln\left(\frac{I_{D1}}{I_s}\right) - V_t \ln\left(\frac{I_{D2}}{I_s}\right) \\ &= V_t \ln\left(\frac{I_{D1}}{I_{D2}}\right) = \frac{kT}{e} \ln\left(\frac{I_{D1}}{I_{D2}}\right) \end{aligned}$$

Hence, the temperature dependence of I_s has been eliminated from the equation.

(b) If I_1 is set to 10 times I_2, then

$$V_{PTAT} = V_t \ln\left(\frac{I_{D1}}{I_{D2}}\right) = \frac{1.38 \times 10^{-23} T}{1.6 \times 10^{-19}} \ln(10) \approx 0.2T \text{ mV}$$

Hence, the voltage is linearly proportional to temperature.

2-17. In this problem, we would like to study the transient characteristics of a *pn*-junction diode. Referring to the circuit shown in Figure 2.35(a), use SPICE to verify the transition characteristic given in Figure 2.35(b). Assume that the diode parameters are as follows:

```
.model Diode D IS=1.0E-15 TT=10E-9 CJO=1E-12 VJ=0.7 M=0.33
```

Solution: A sample SPICE program is as follows:

```
A study of pn Diode transition characteristics  ——
********** Parameters and model **********
.model Diode D IS=1.0E-15 TT=10E-9 CJO=1E-12 VJ=0.7 M=0.33
******** Circuit description **********
```

```
D1  Vd 0 Diode
R1  Vin vd 1k
Vin vin 0 DC 0 pulse 5 −5 10n 0.1n 0.1n 20n 40n
********* Analysis statement ************
.tran 100p 50n
********* Output statements *************
.print i(Vin) PAR('−i(Vin)*1k')
.END
```

2-18. Referring to Figure 1.33(a), design a two-stage buffer. The first stage is a standard $1X$ inverter and the second stage is a $4X$ inverter. Assume that $L = 2\lambda$ and $W = 3\lambda$.

Solution: A sample SPICE program is as follows:

```
A two−stage buffer design —— 0.18−um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
******** Circuit description **********
Mn1    a Vin Gnd Gnd nmos L=2 W=3  ** input stage
Mp1    a Vin Vdd Vdd pmos L=2 W=6
Mn2 Vout   a Gnd Gnd nmos L=2 W=12 ** output stage
Mp2 Vout   a Vdd Vdd pmos L=2 W=24
Vdd Vdd  Gnd 'Supply'
Vin Vin  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
******** analysis statement *******
.trans 1ps 4ns 10ps
******** Output statements *******
.probe V(Vin) V(Vout)
.END
```

2-19. Referring to Figure 1.33(b), write a SPICE data file to verify the function of the two-input NAND gate. Assume that $L = 2\lambda$ and $W = 3\lambda$.

Solution: A sample SPICE program is as follows:

```
A two−input NAND gate —— 0.18−um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
******** Circuit description **********
Mn1     x   B Gnd Gnd nmos L=2 W=6 ** input B
Mn2  Vout   A   x Gnd nmos L=2 W=6 ** input A
Mp1  Vout   B Vdd Vdd pmos L=2 W=6
Mp2  Vout   A Vdd Vdd pmos L=2 W=6
Vdd  Vdd  Gnd 'Supply'
VinA   A  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
VinB   B  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 2ns 4ns
******** analysis statement *******
.trans 1ps 4ns 10ps
******** Output statements *******
.probe V(VinA) V(VinB) V(Vout)
.END
```

2-20. Referring to Figure 1.33(c), write a SPICE data file to verify the function of the two-input NOR gate. Assume that $L = 2\lambda$ and $W = 3\lambda$.

Solution: A sample SPICE program is as follows:

```
A two-input NOR gate ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
******** Circuit description **********
Mn1  Vout   B Gnd Gnd nmos L=2 W=3 ** input B
Mn2  Vout   A Gnd Gnd nmos L=2 W=3 ** input A
Mp1  Vout   B   x Vdd pmos L=2 W=12
Mp2     x   A Vdd Vdd pmos L=2 W=12
Vdd   Vdd Gnd 'Supply'
VinA    A Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
VinB    B Gnd PULSE 0 'Supply' 0ps 0ps 0ps 2ns 4ns
******** analysis statement *******
.trans 1ps 4ns 10ps
******** Output statements *******
.probe V(VinA) V(VinB) V(Vout)
.END
```

2-21. Referring to Figure 1.35(a), write a SPICE data file to verify the function of the 2-to-1 multiplexer. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A 2-to-1 nMOS multiplexer ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
******** Circuit description **********
Mn1     Y Sbar  D0 Gnd nmos L=2 W=3 ** input D0
Mn2     Y    S  D1 Gnd nmos L=2 W=3 ** input D1
Mn3  Sbar    S Gnd Gnd nmos L=2 W=3
Mp3  Sbar    S Vdd Vdd pmos L=2 W=3
Vdd   Vdd  Gnd 'Supply'
VinD0  D0  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
VinD1  D1  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 2ns 4ns
VinS    S  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 3ns 6ns
******** analysis statement *******
.trans 1ps 6ns 10ps
******** Output statements *******
.probe V(VinD0) V(VinD1) V(VinS) V(Y)
.END
```

2-22. Referring to Figure 1.35(b), define a sub-circuit of TG and write a SPICE data file to verify the function of the 2-to-1 multiplexer. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A 2-to-1 TG multiplexer ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
********** Subcircuit definition **********
.global vdd gnd
.subckt TG a y nctrl pctrl
Mn y nctrl a gnd nmos L=2 W=3
Mp y pctrl a vdd pmos L=2 W=3
.ends
** define an inverter
.subckt inv a y *** a=input y=output
Mn y a gnd gnd nmos L=2 W=3
Mp y a vdd vdd pmos L=2 W=3
.ends
******** Circuit description **********
XTG1  D0    Y Sbar    S TG ** input D0
XTG2  D1    Y    S Sbar TG ** input D1
Xinv   S Sbar inv          ** inverter
Vdd   Vdd  Gnd 'Supply'
VinD0  D0  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
VinD1  D1  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 2ns 4ns
VinS    S  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 3ns 6ns
******** analysis statement *******
.trans 1ps 6ns 10ps
******** Output statements *******
.probe V(VinD0) V(VinD1) V(VinS) V(Y)
.END
```

2-23. Referring to Figure 1.36(a), write a SPICE data file to verify the function of the 1-to-2 demultiplexer. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A 1-to-2 nMOS demultiplexer ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
******** Circuit description **********
Mn1     D Sbar  Y0 Gnd nmos L=2 W=3 ** input D0
Mn2     D    S  Y1 Gnd nmos L=2 W=3 ** input D1
Mn3  Sbar    S Gnd Gnd nmos L=2 W=3
Mp3  Sbar    S Vdd Vdd pmos L=2 W=3
Vdd   Vdd  Gnd 'Supply'
VinD    D  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
VinS    S  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 3ns 6ns
******** analysis statement *******
.trans 1ps 6ns 10ps
******** Output statements *******
.probe V(VinD) V(VinS) V(Y0) V(Y1)
.END
```

2-24. Referring to Figure 1.36(b), define a sub-circuit of TG and write a SPICE data file to verify the function of the 1-to-2 demultiplexer. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A 1-to-2 TG demultiplexer ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
********** Subcircuit definition **********
.global vdd gnd
.subckt TG a y nctrl pctrl
Mn y nctrl a gnd nmos L=2 W=3
Mp y pctrl a vdd pmos L=2 W=3
.ends
** define an inverter
.subckt inv a y *** a=input y=output
Mn y a gnd gnd nmos L=2 W=3
Mp y a vdd vdd pmos L=2 W=3
.ends
******** Circuit description **********
XTG1   D   Y0 Sbar    S TG ** output Y0
XTG2   D   Y1    S Sbar TG ** output Y1
Xinv   S Sbar inv          ** inverter
Vdd   Vdd  Gnd 'Supply'
VinD    D  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
VinS    S  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 3ns 6ns
******** analysis statement *******
.trans 1ps 20ns 10ps
******** Output statements *******
.probe V(VinD) V(VinS) V(Y0) V(Y1)
.END
```

2-25. Referring to Figure 1.37(a), define a sub-circuit of TG and write a SPICE data file to verify the function of the positive D-type latch. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A positive D-type latch ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
********** Subcircuit definition **********
.global vdd gnd
.subckt TG a y nctrl pctrl
Mn y nctrl a gnd nmos L=2 W=3
Mp y pctrl a vdd pmos L=2 W=3
.ends
** define an inverter
.subckt inv a y *** a=input y=output
Mn y a gnd gnd nmos L=2 W=3
Mp y a vdd vdd pmos L=2 W=3
```

```
.ends
******** Circuit description **********
XTG1      D    l clk  clkb TG ** S1
XTG2      x    l clkb  clk TG ** S2
Xinv1     l Qbar inv    ** output inverter
Xinv2  Qbar    x inv    ** feedback inverter
Xinv3   clk clkb inv    ** clkb geberator
Vdd   Vdd  Gnd 'Supply'
VinD    D  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
Vclk  clk  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 3ns 6ns
******** analysis statement *******
.trans 1ps 20ns 10ps
******** Output statements *******
.probe V(VinD) V(Vclk) V(Qbar)
.END
```

2-26. Referring to Figure 1.37(b), define a sub-circuit of TG and write a SPICE data file to verify the function of the negative D-type latch. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A negative D-type latch ---- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
********** Subcircuit definition **********
.global vdd gnd
.subckt TG a y nctrl pctrl
Mn y nctrl a gnd nmos L=2 W=3
Mp y pctrl a vdd pmos L=2 W=3
.ends
** define an inverter
.subckt inv a y *** a=input y=output
Mn y a gnd gnd nmos L=2 W=3
Mp y a vdd vdd pmos L=2 W=3
.ends
******** Circuit description **********
XTG1      D    l clkb  clk TG ** S1
XTG2      x    l  clk clkb TG ** S2
Xinv1     l Qbar inv    ** output inverter
Xinv2  Qbar    x inv    ** feedback inverter
Xinv3   clk clkb inv    ** clkb geberator
Vdd   Vdd  Gnd 'Supply'
VinD    D  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 1ns 2ns
Vclk  clk  Gnd PULSE 0 'Supply' 0ps 0ps 0ps 3ns 6ns
******** analysis statement *******
.trans 1ps 20ns 10ps
******** Output statements *******
.probe V(VinD) V(Vclk) V(Qbar)
.END
```

2-27. Referring to Figure 1.38, define a sub-circuit of D-type latch and write a SPICE data file to verify the

function of the master-slave positive-edge triggered D-type flip-flop. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A positive-edge triggered D-type FF --- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
********** Subcircuit definition **********
.global vdd gnd
*** define a TG switch ***
.subckt TG a y nctrl pctrl
Mn y nctrl a gnd nmos L=2 W=3
Mp y pctrl a vdd pmos L=2 W=3
.ends
*** define an inverter ***
.subckt inv a y *** a=input y=output
Mn y a gnd gnd nmos L=2 W=3
Mp y a vdd vdd pmos L=2 W=3
.ends
*** define a D-type latch ***
.subckt Dlatch D Qbar clk clkb ***
XTG1      D    l  clk clkb TG ** S1
XTG2      x    l clkb  clk TG ** S2
Xinv1     l Qbar  inv ** output inverter
Xinv2  Qbar    x  inv ** feedback inverter
.ends
******** Circuit description *********
XMaster      D Qmaster clkn clkb Dlatch ** master latch
XSlave Qmaster  Qslave clkb clkn Dlatch ** slave latch
Xinv1      clk    clkn  inv        ** clkn geberator
Xinv2     clkn    clkb  inv        ** clkb geberator
Vdd  Vdd Gnd 'Supply'
VinD   D Gnd PULSE 0 'Supply' 0ps 0ps 0ps 4ns 6ns
Vclk  clk  Gnd PULSE 0 'Supply' 0ns 0ps 0ps 7ns 11ns
******** analysis statement *******
.trans 1ps 40ns 10ps
******** Output statements *******
.probe V(VinD) V(Vclk) V(Qslave)
.END
```

2-28. Referring to Figure 1.38, define a sub-circuit of D-type latch and write a SPICE data file to verify the function of the master-slave negative-edge triggered D-type flip-flop. Assume that $L = 2\lambda$ and $W = 3\lambda$ are used for all transistors.

Solution: A sample SPICE program is as follows:

```
A negative-edge triggered D-type FF --- 0.18-um process
******** Parameters and model *********
.lib   '..\cmos18.txt' cmos
.param Supply=1.8V   * Set value of Vdd
.opt   scale=0.09u
```

```
********** Subcircuit definition **********
.global vdd gnd
*** define a TG switch ***
.subckt TG a y nctrl pctrl
Mn y nctrl a gnd nmos L=2 W=3
Mp y pctrl a vdd pmos L=2 W=3
.ends
*** define an inverter ***
.subckt inv a y *** a=input y=output
Mn y a gnd gnd nmos L=2 W=3
Mp y a vdd vdd pmos L=2 W=3
.ends
*** define a D-type latch ***
.subckt Dlatch D Qbar clk clkb ***
XTG1      D    1  clk clkb TG ** S1
XTG2      x    1 clkb  clk TG ** S2
Xinv1     1 Qbar  inv ** output inverter
Xinv2  Qbar    x  inv ** feedback inverter
.ends
******** Circuit description *********
XMaster      D Qmaster clkb clkn Dlatch ** master latch
XSlave Qmaster  Qslave clkn clkb Dlatch ** slave latch
Xinv1      clk    clkn  inv        ** clkn geberator
Xinv2     clkn    clkb  inv        ** clkb geberator
Vdd  Vdd Gnd 'Supply'
VinD   D Gnd PULSE 0 'Supply' 0ps 0ps 0ps 4ns 6ns
Vclk  clk  Gnd PULSE 0 'Supply' 0ns 0ps 0ps 7ns 11ns
******** analysis statement *******
.trans 1ps 40ns 10ps
******** Output statements *******
.probe V(VinD) V(Vclk) V(Qslave)
.END
```