FIGURE 2.1

(a) Covalent bonding of the silicon atom. (b) Energy-band diagram of an intrinsic silicon crystal.

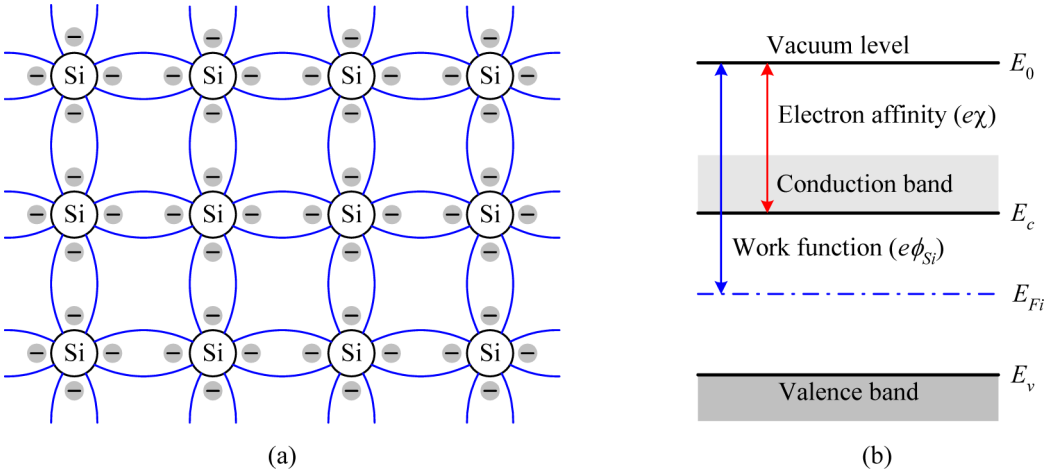


FIGURE 2.2

(a) Covalent bonding of boron impurity in *p*-type silicon. (b) Energy-band diagram of a *p*-type silicon semiconductor.

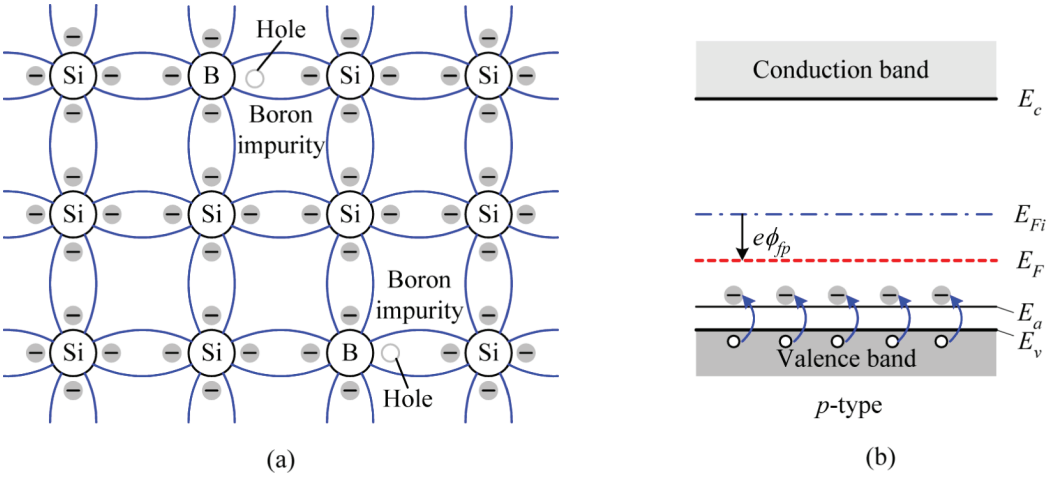


FIGURE 2.3

(a) Covalent bonding of antimony impurity in an *n*-type silicon. (b) Energy-band diagram of an *n*-type silicon semiconductor.

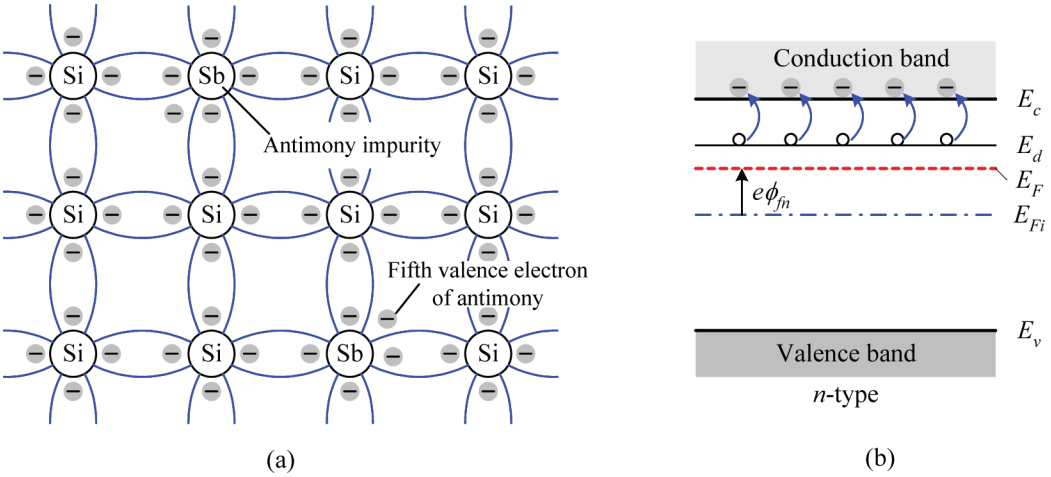


FIGURE 2.4

The drift current model of a conductor in an electric field.

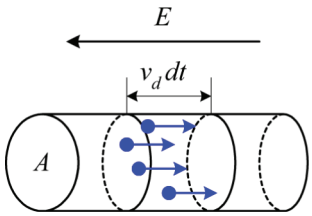


FIGURE 2.5

The *pn* and metal-semiconductor junctions in a CMOS inverter.

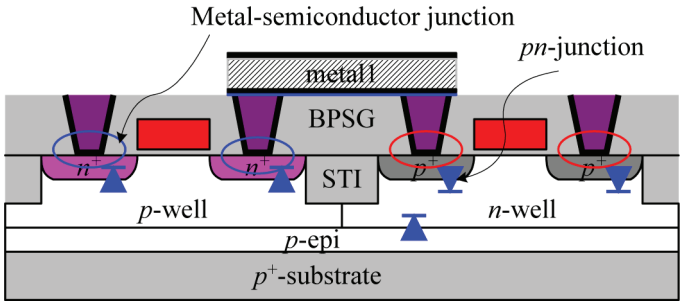


FIGURE 2.6

The (a) basic structure and (b) depletion region of a *pn*-junction.

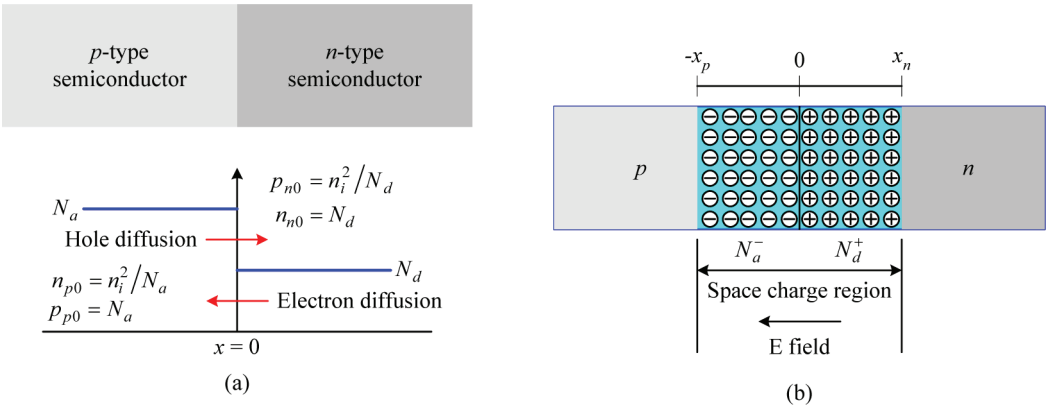


FIGURE 2.7

The energy-band diagrams of a typical *pn*-junction (a) before and (b) after combination.

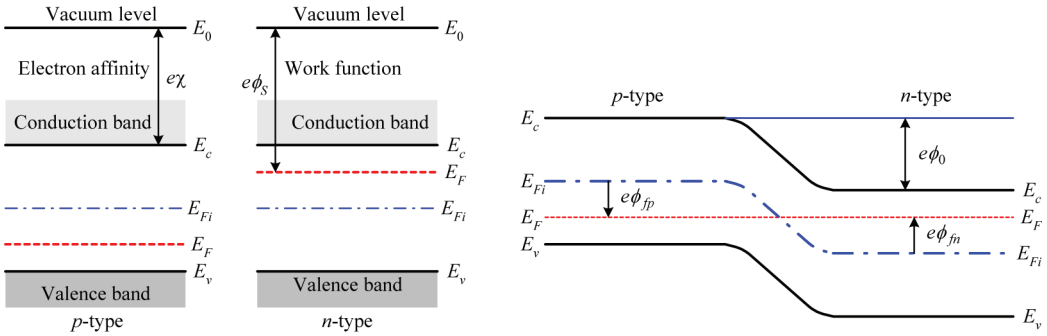
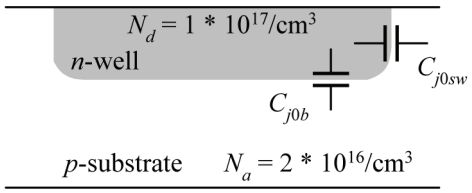
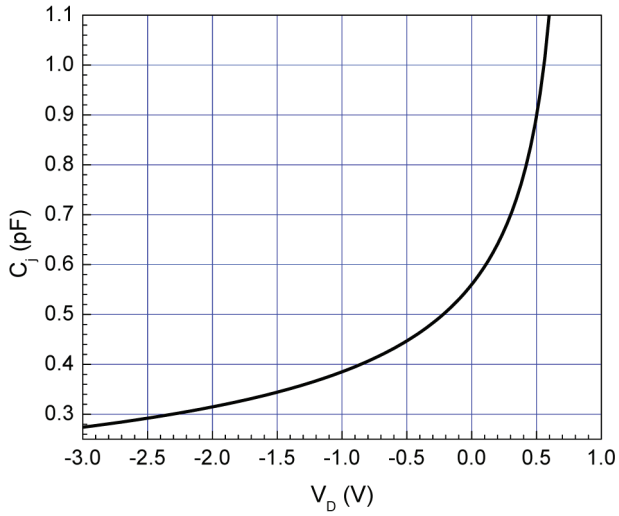


FIGURE 2.8

(a) The structure of an *n*-well junction. (b) The *pn*-junction capacitance between an *n*-well and the *p*-substrate.



(a)



(b)

FIGURE 2.9

The (a) structure and (b) energy-band diagram of a basic MOS system.

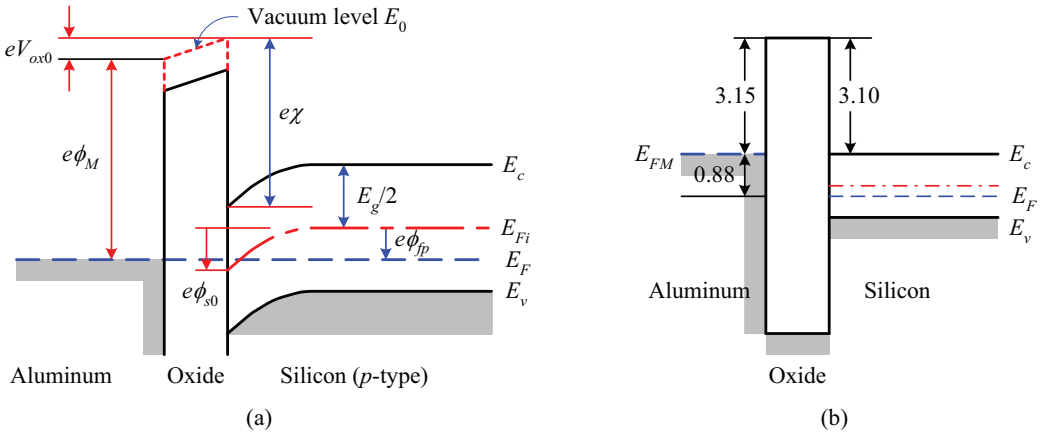


FIGURE 2.10

(a) An energy-band diagram showing the definition of surface potential. (b) The energy-band diagram of flat-band voltage.

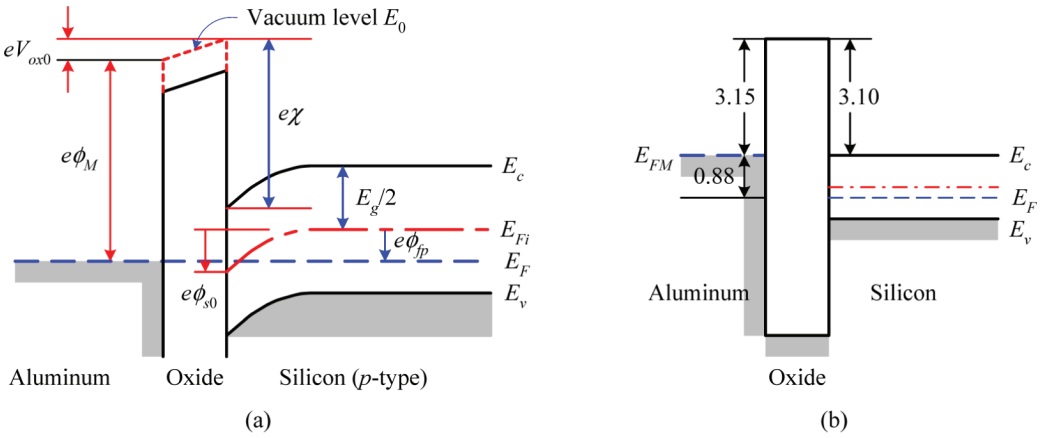


FIGURE 2.11

An ideal MOS system with a *p*-type substrate with various operation modes: (a) flat band; (b) accumulation; (c) depletion; (d) inversion.

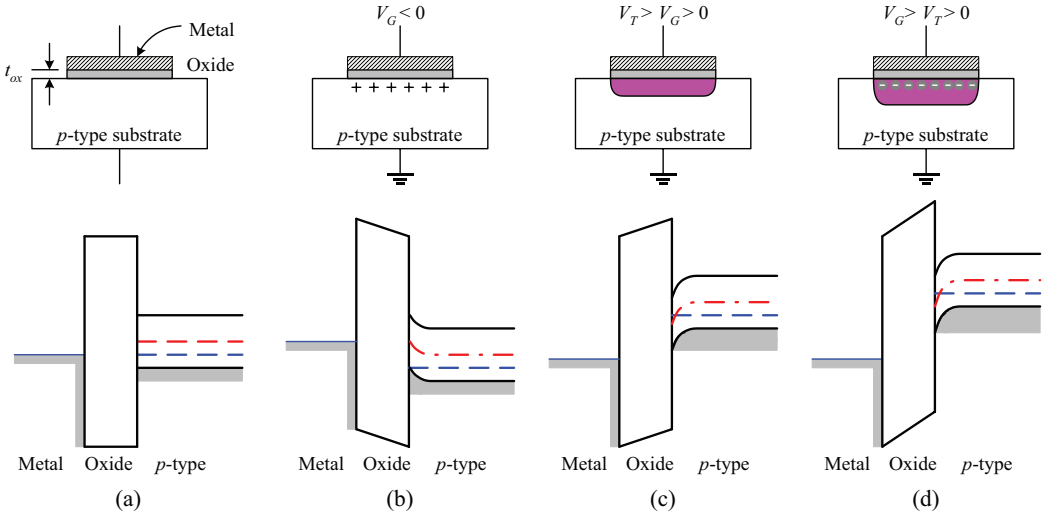


FIGURE 2.12

The definition of threshold voltages of ideal MOS systems with both (a) *p*-type and (b) *n*-type substrates, respectively.

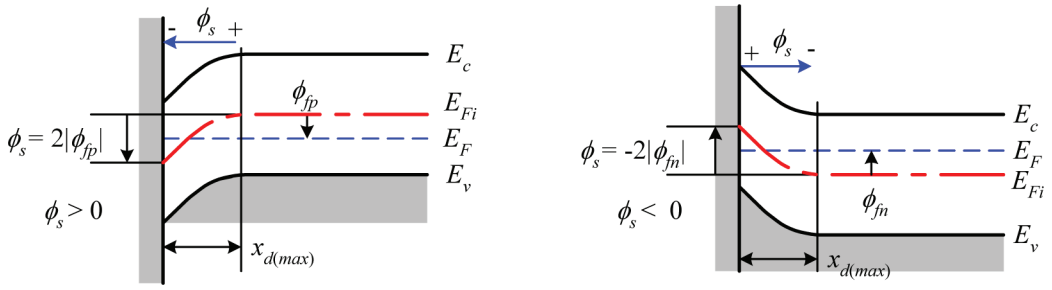


FIGURE 2.13

The cutoff mode of an nMOS transistor.

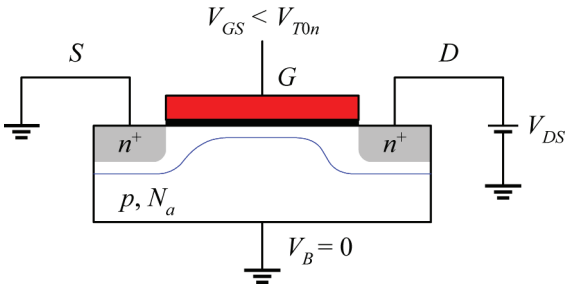


FIGURE 2.14

The linear mode of an nMOS transistor.

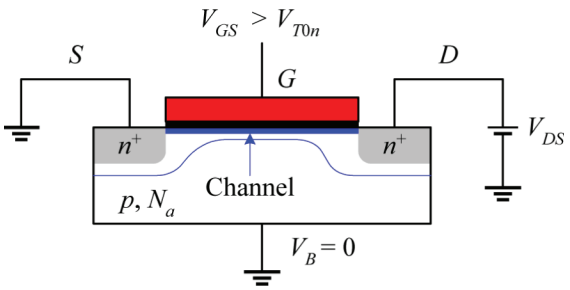


FIGURE 2.15

The saturation mode of an nMOS transistor.

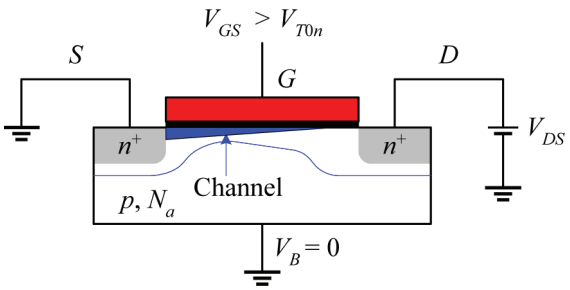


FIGURE 2.16

The (a) GCA model and (b) derived *I-V* characteristics of an nMOS transistor.

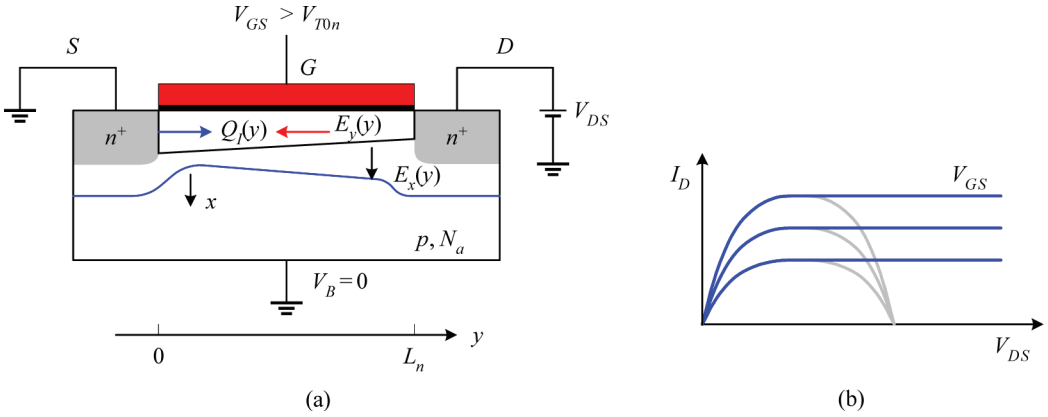


FIGURE 2.17

The typical characteristics of (a) nMOS and (b) pMOS transistors.

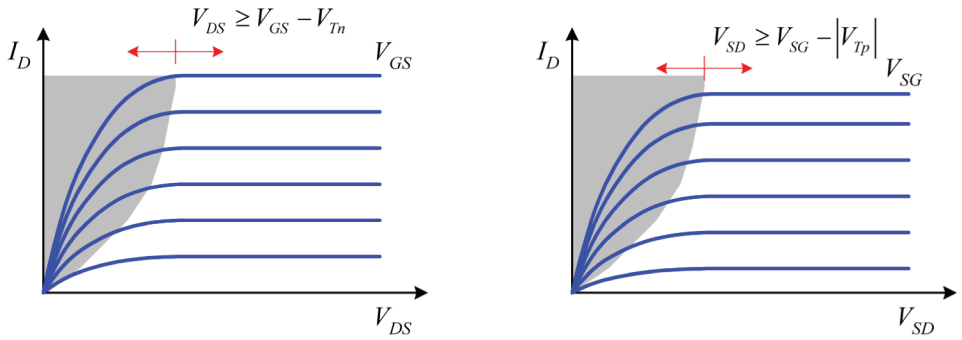
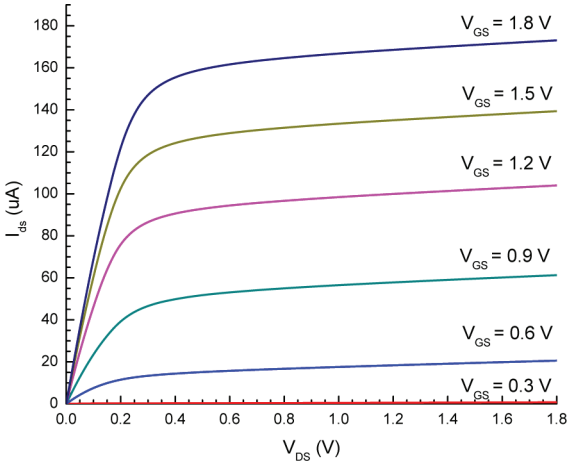
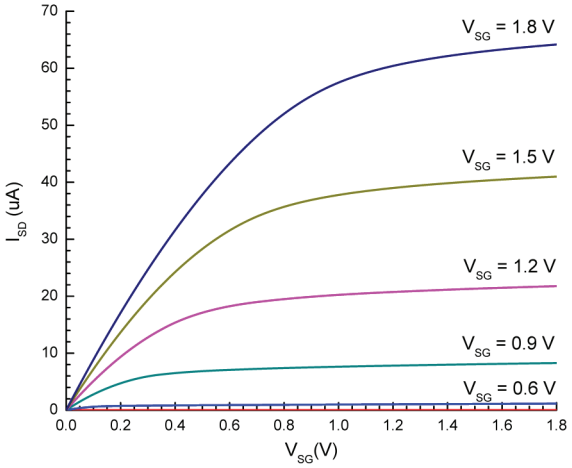


FIGURE 2.18

The *I-V* characteristics of (a) nMOS and (b) pMOS transistors.



(a)



(b)

FIGURE 2.19

A conceptual illustration of scaling theory: (a) original; (b) scaled.

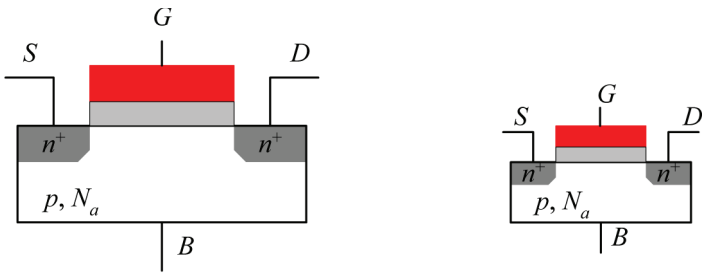


FIGURE 2.20

The effect of channel-length modulation of an nMOS transistor.

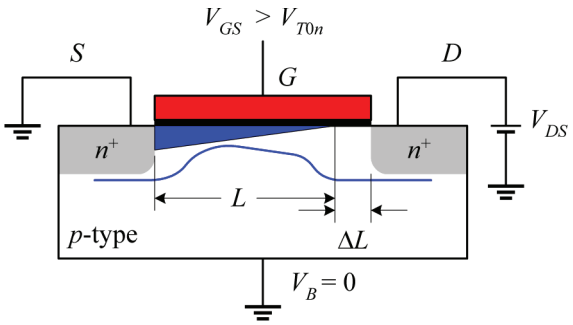


FIGURE 2.21

An illustration of velocity saturation of electrons and holes in a silicon semiconductor.

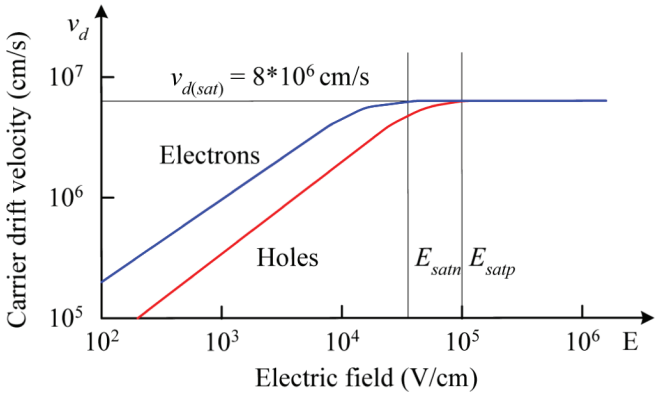


FIGURE 2.22

A cross-sectional view of a lightly-doped drain (LDD) CMOS transistor.

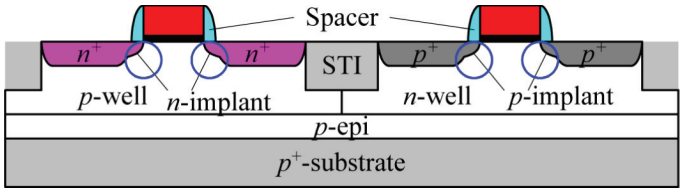
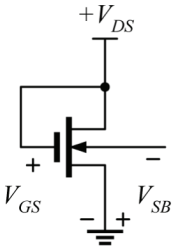
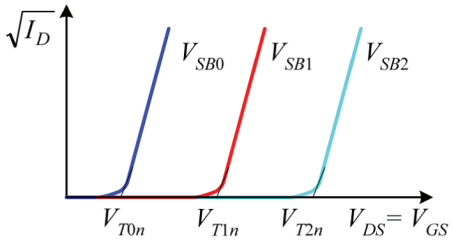


FIGURE 2.23

The body effects of a typical nMOS transistor: (a) circuit; (b) *I-V* characteristics.



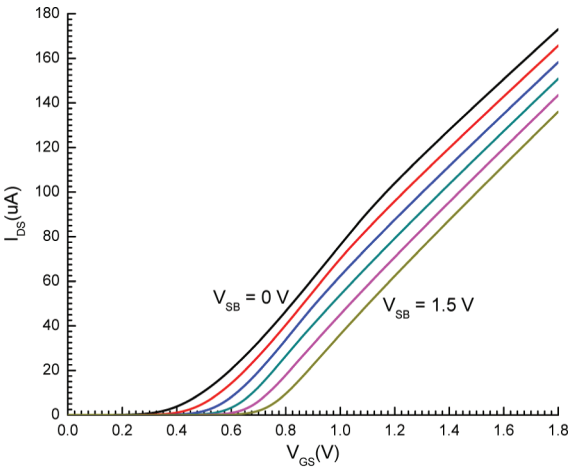
(a)



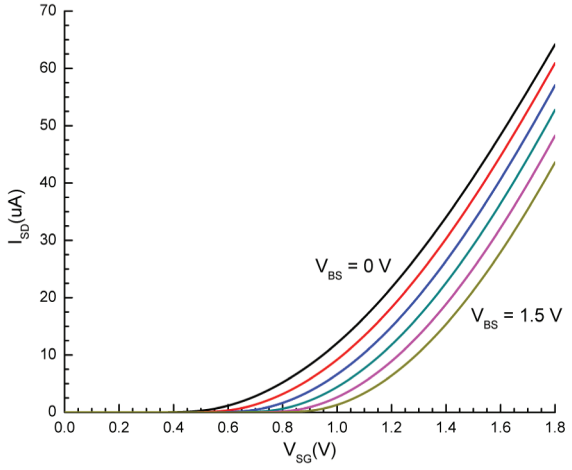
(b)

FIGURE 2.24

The body effects of (a) nMOS and (b) pMOS transistors.



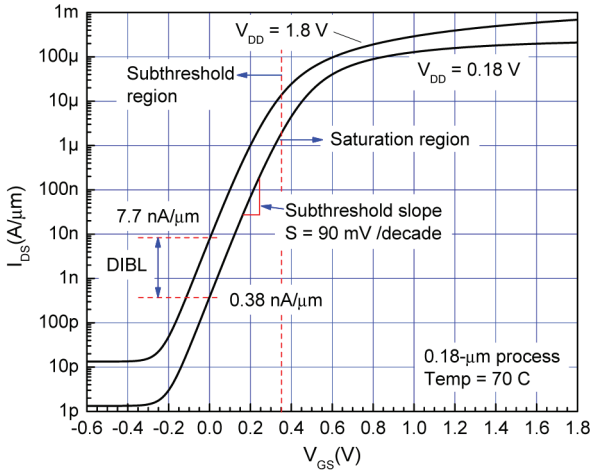
(a)



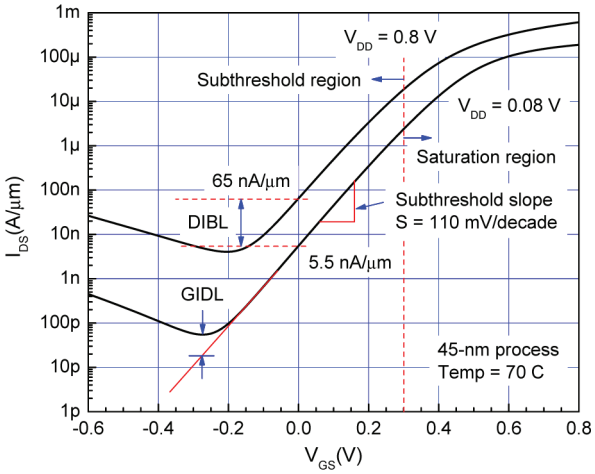
(b)

FIGURE 2.25

The subthreshold currents of (a) a 0.18-μm and (b) a 45-nm nMOS transistors at 70°C.



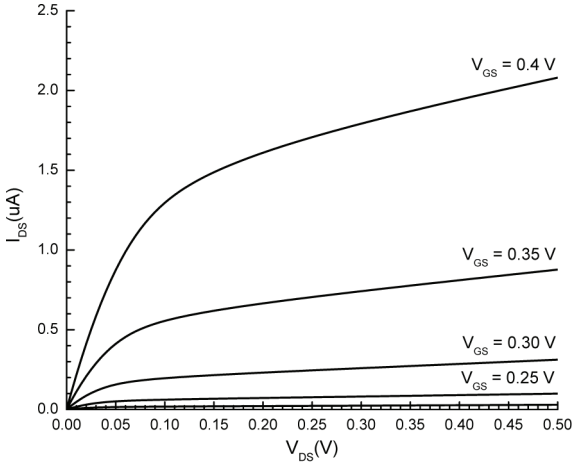
(a)



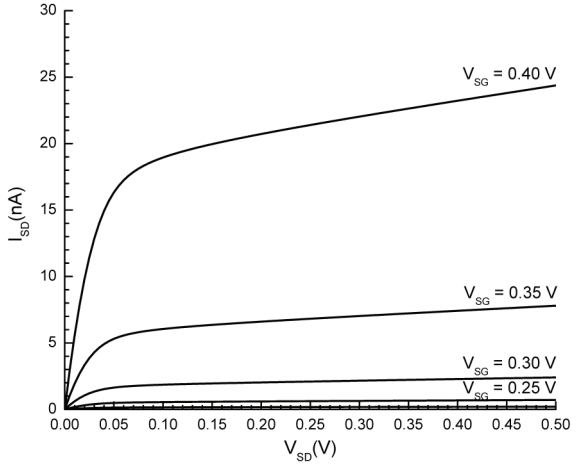
(b)

FIGURE 2.26

The current-voltage characteristics of (a) nMOS and (b) pMOS transistors in subthreshold regions.



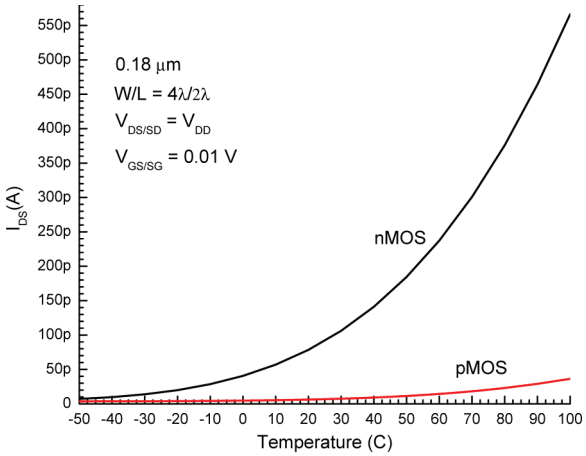
(a)



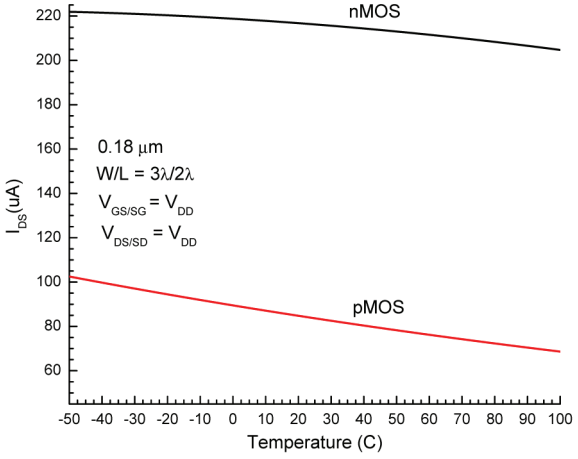
(b)

FIGURE 2.27

The temperature effects on the current-voltage characteristics of MOS transistors: (a) low V_{GS}; (b) $V_{GS} = V_{DD}$.



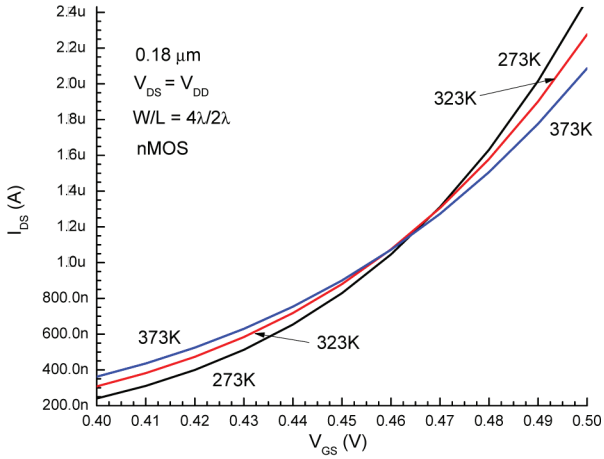
(a)



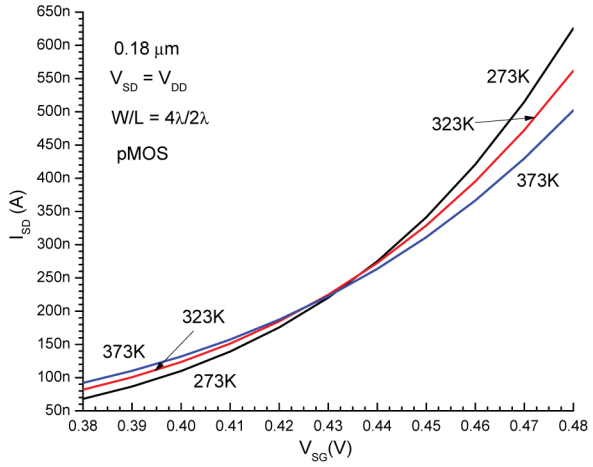
(b)

FIGURE 2.28

The detailed temperature effects on the current-voltage characteristics of MOS transistors: (a) nMOS transistor; (b) pMOS transistor.



(a)



(b)

FIGURE 2.29

Examples of (a) voltage and (b) current sources.


```
Vsupply Vdd Gnd +3V
```

(a)

```
Isupply 3 0 1mA
```

(b)

FIGURE 2.30

The specifications of a pulse source.

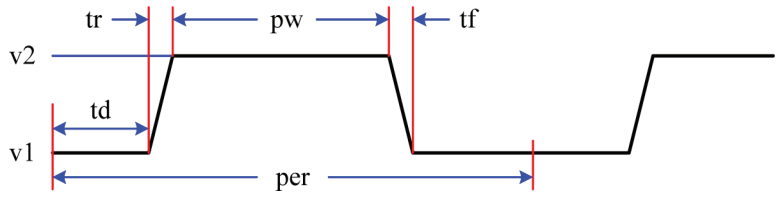


FIGURE 2.31

The specifications of the areas and perimeters of connected MOS transistors: (a) isolated contacted source/drain; (b) contacted source/drain sharing; (c) uncontacted source/drain sharing.

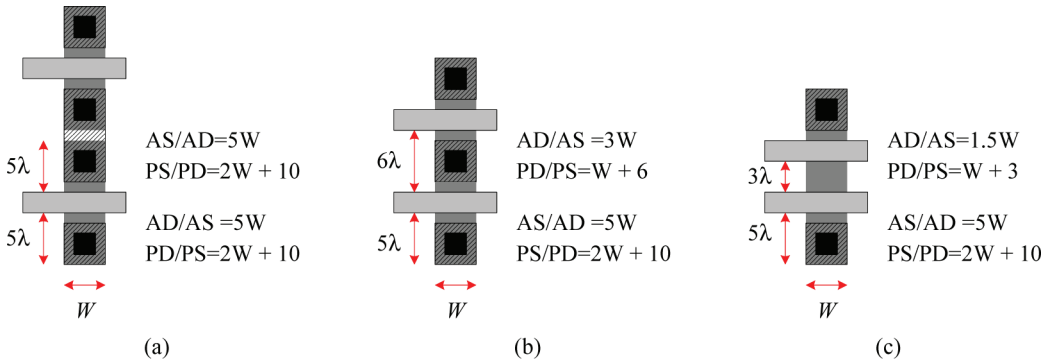


FIGURE 2.32

SPICE model of a typical *pn*-junction diode.

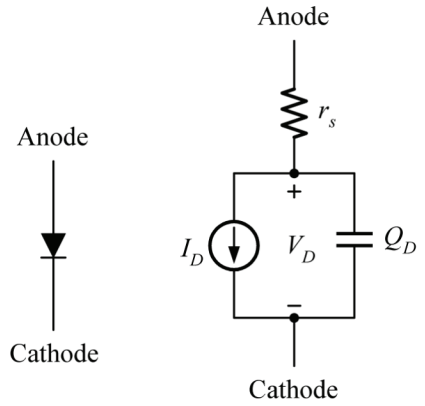


FIGURE 2.33

The concept of a binning process.

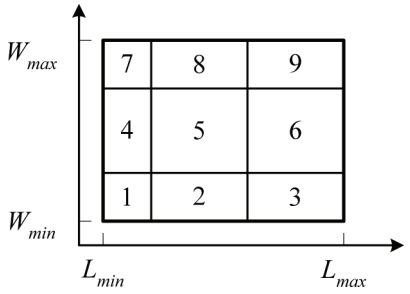


FIGURE 2.34

The circuit of PTAT.

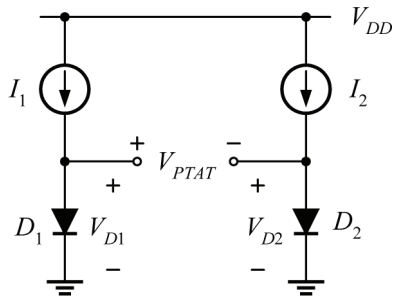


FIGURE 2.35

The (a) circuit of a *pn*-junction diode for studying (b) transition characteristic.