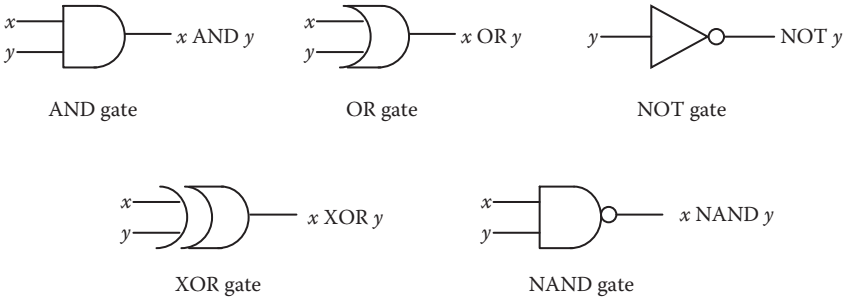

Figure 1.1
Symbols for logic gates.

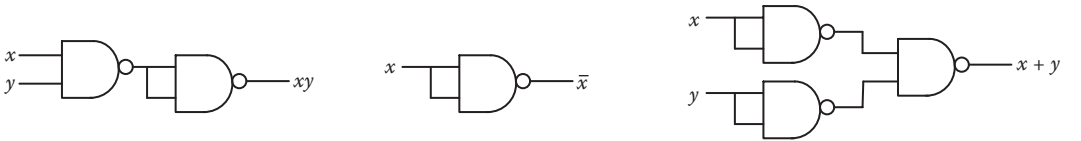

Figure 1.2
Construction of the AND, NOT, and OR gates, using only the NAND gates.

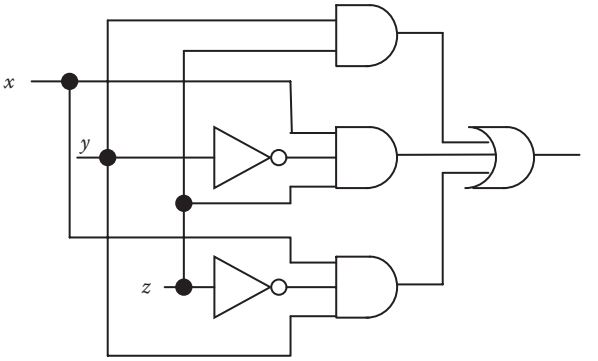

Figure 1.3
Logic diagram for $yz + x\bar{y}z + xy\bar{z}$.

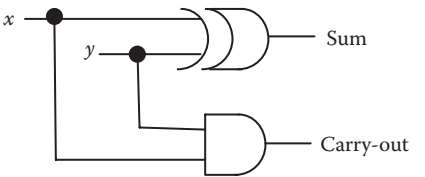

Figure 1.4
Logic diagram of the digital logic circuit for the 1-bit half adder.

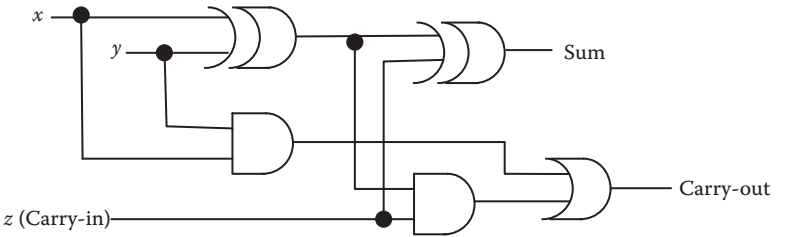

Figure 1.5
Logic diagram of the digital logic circuit for the 1-bit full adder.

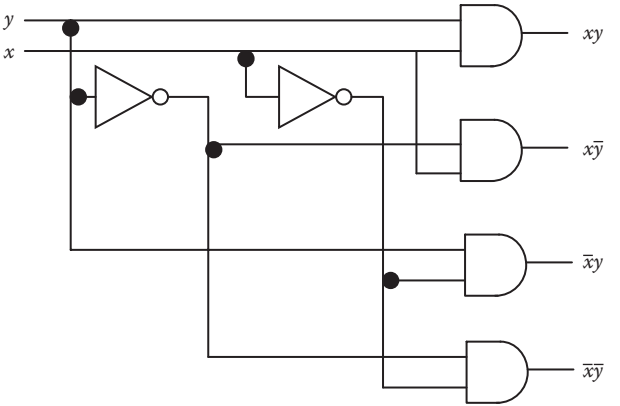

Figure 1.6
Logic diagram of the digital logic circuit for a 2- to 4-bit decoder.

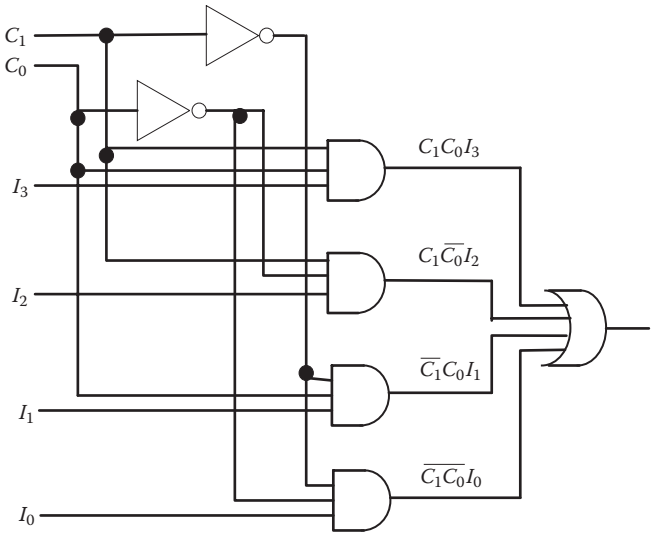

Figure 1.7
Logic diagram of the digital logic circuit for a multiplexer.

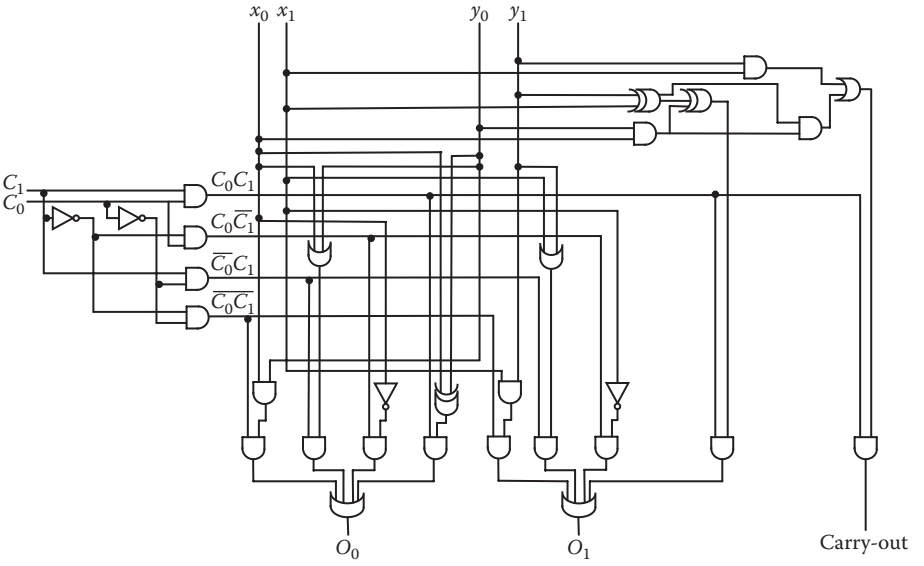

Figure 1.8
Logic diagram of the digital logic circuit for a simple ALU.

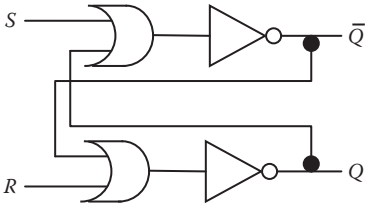

Figure 1.9
SR flip-flop without clock.

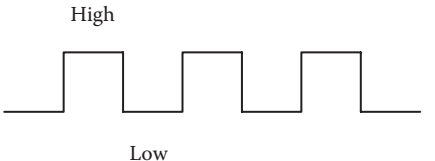

Figure 1.10
Clock signal with a series of pulses.

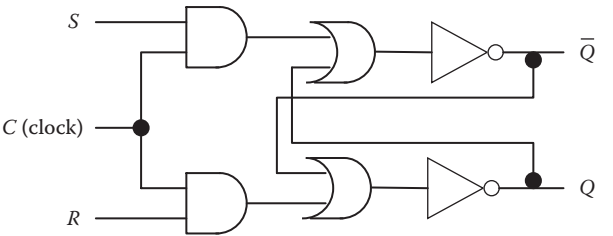

Figure 1.11
SR flip-flop with clock.

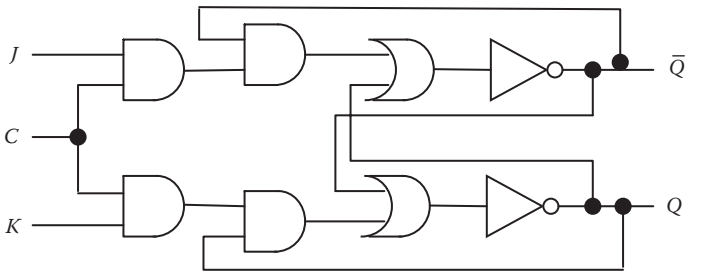

Figure 1.12
JK flip-flop with clock.

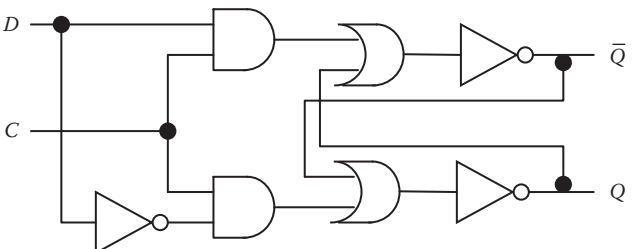

Figure 1.13
D flip-clop with clock.

001x013.eps

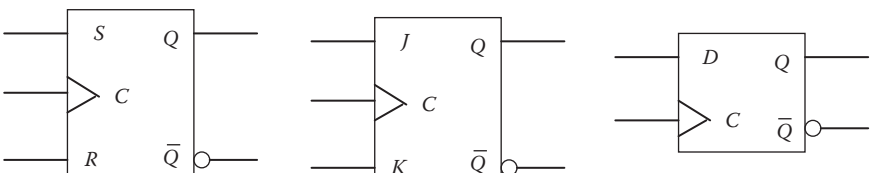

Figure 1.14
Logic diagram symbols for the SR, JK, and D flip-flops.

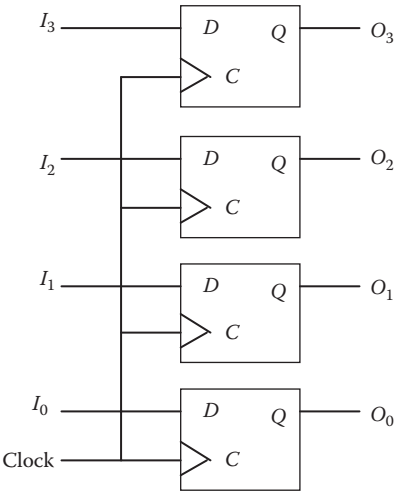

Figure 1.15
Logic diagram of the sequential circuit for a 4-bit register.

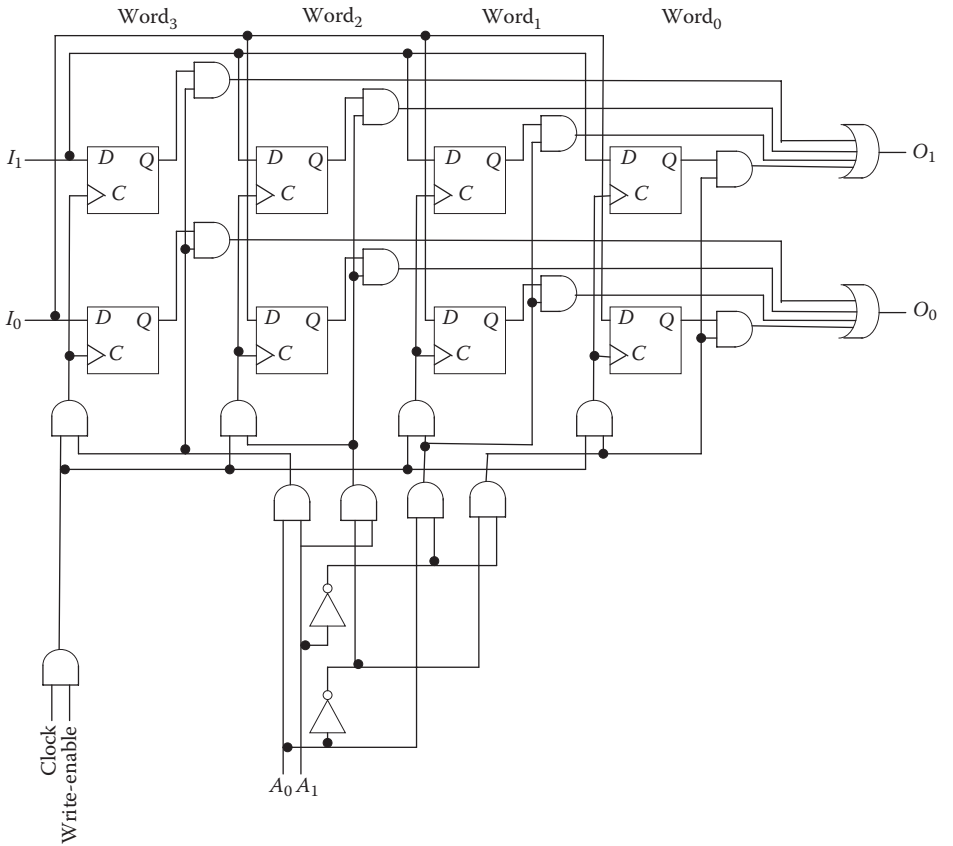

Figure 1.16
Logic diagram of the sequential circuit for a 2-bit memory to store four words.