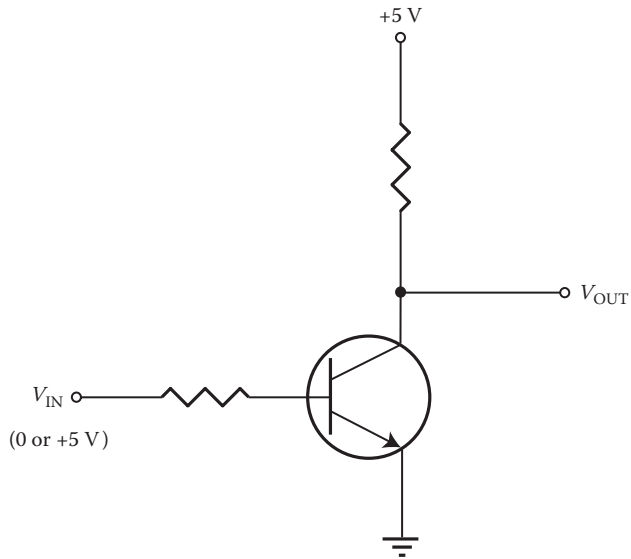Figure 2.1
Ideal diode.

Figure 2.2
An example of a transistor inverter.
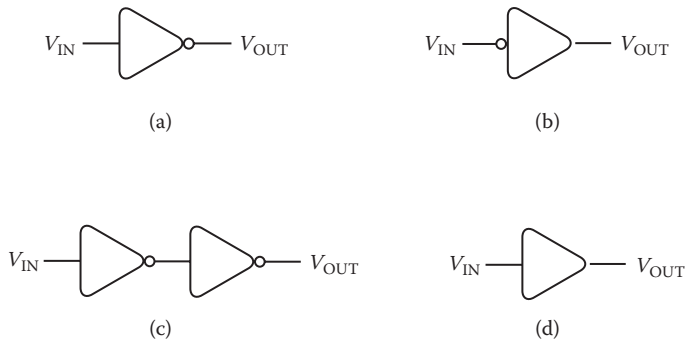
Figure 2.3
Logic symbols: (a) active-HIGH input inverter, (b) active-LOW input inverter, (c) double inverter, (d) buffer.

002x003.eps

High (1)

Low (0)

t_1 t_2

Input Pulse

High (1)

Low (0)
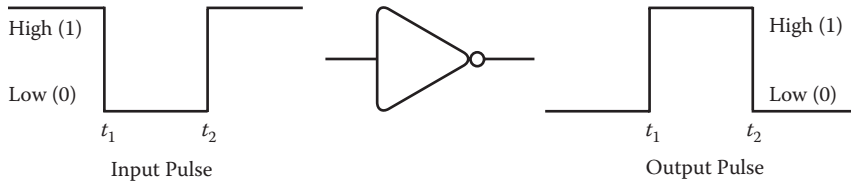
t_1 t_2

Output Pulse
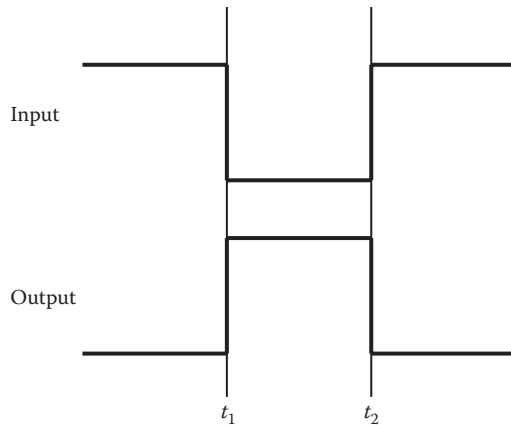
Figure 2.4
Inverter operation with a pulse input.

Figure 2.5
Timing diagram for Figure 2.4.
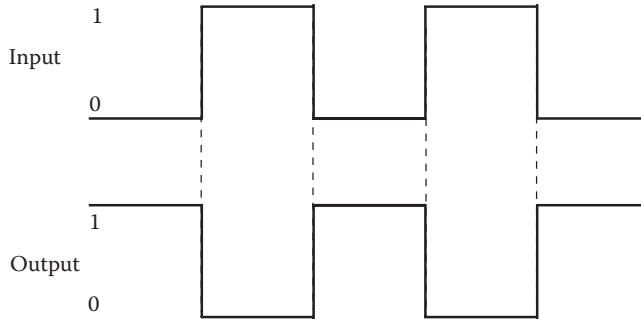
Figure 2.6
Timing diagram for Example 2.1.

Figure 2.7
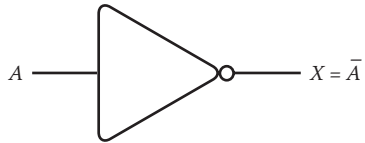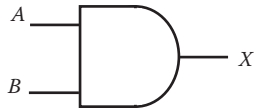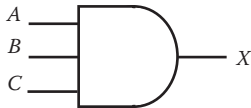Timing diagram solution for Example 2.1.

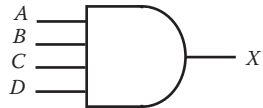Figure 2.8
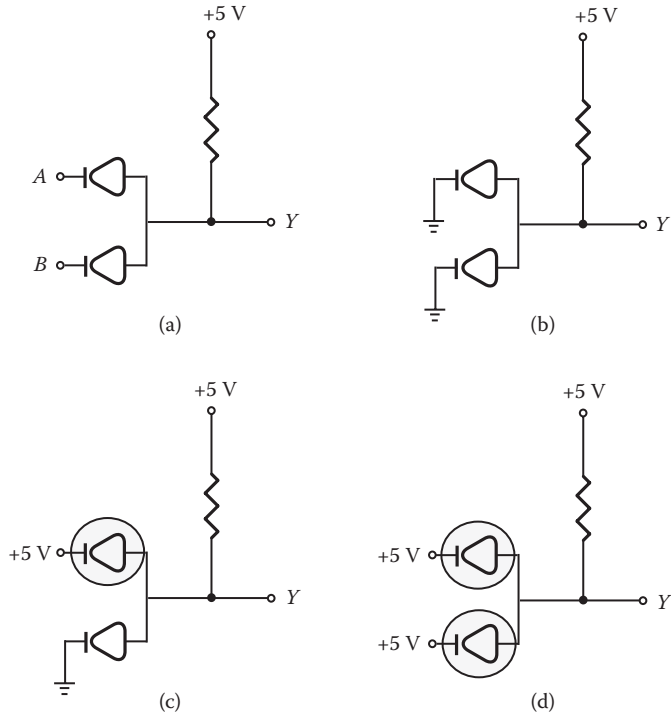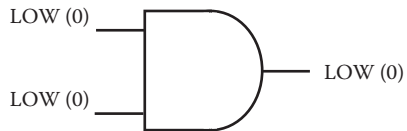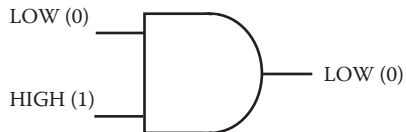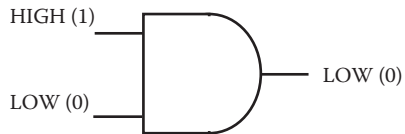Logic expressions for an inverter.

002x008.eps

Figure 2.9
AND gate symbols.

Figure 2.10
A simple AND gate construction with various scenarios.
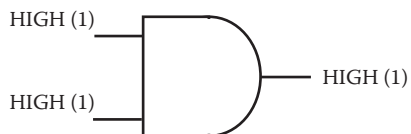
Figure 2.11
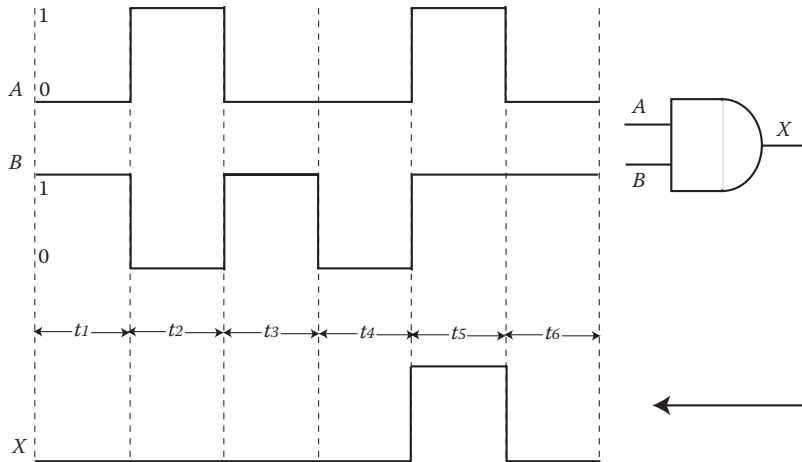Operation of a 2-input AND gate.

Figure 2.12
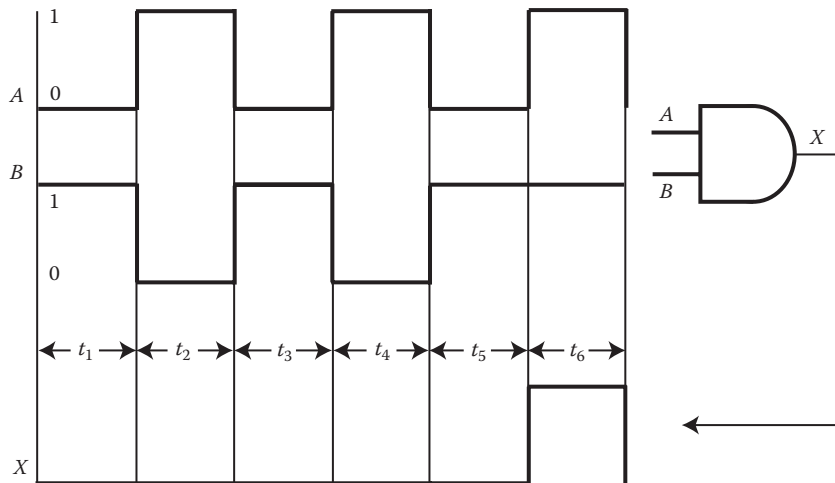Example of an AND Gate operation with a timing diagram showing input and output relationships.
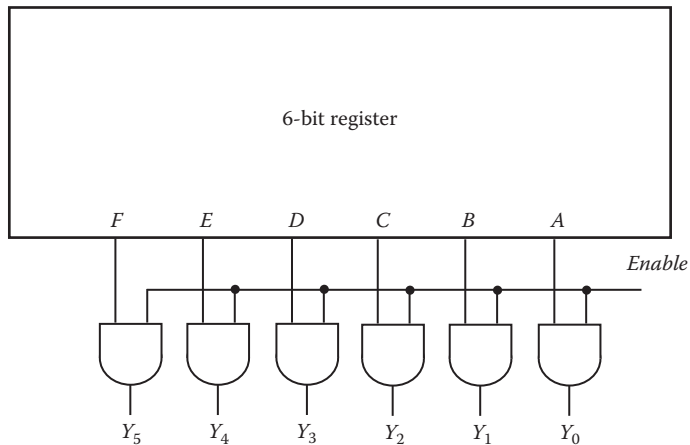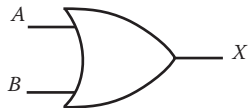
002x012.eps

Figure 2.13
Timing diagram for a 2-input AND gate.

Figure 2.14
Using AND gates to block or transmit data.

Figure 2.15
OR gate symbols.

002x015.eps

LOW (0)

LOW (0)

LOW (0)

(a)

LOW (0)

HIGH (1)

HIGH (1)

(b)

HIGH (1)

LOW (0)

HIGH (1)

(c)

HIGH (1)

HIGH (1)

HIGH (1)
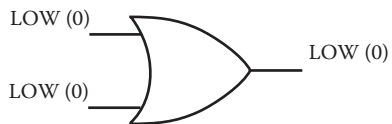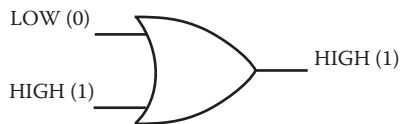
(d)

Figure 2.16
Operation of a 2-input OR gate.

Figure 2.17
A 3-input diode OR gate.

Figure 2.18
Example of OR gate operation with a timing diagram showing input and output relationships.

Figure 2.19
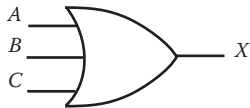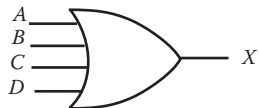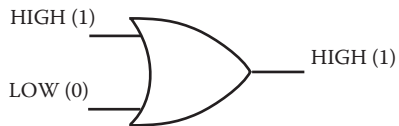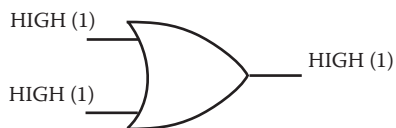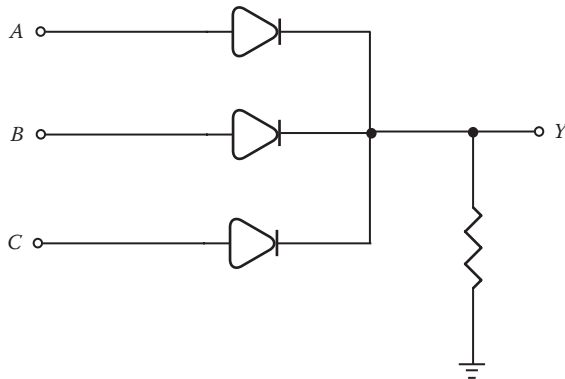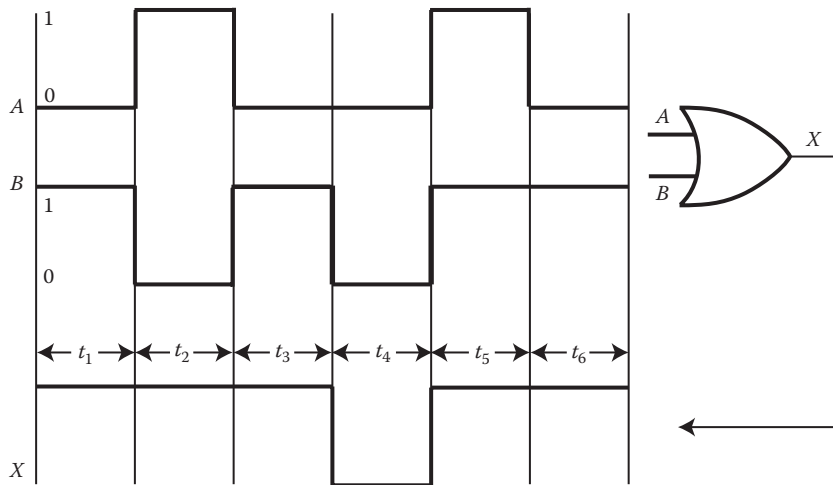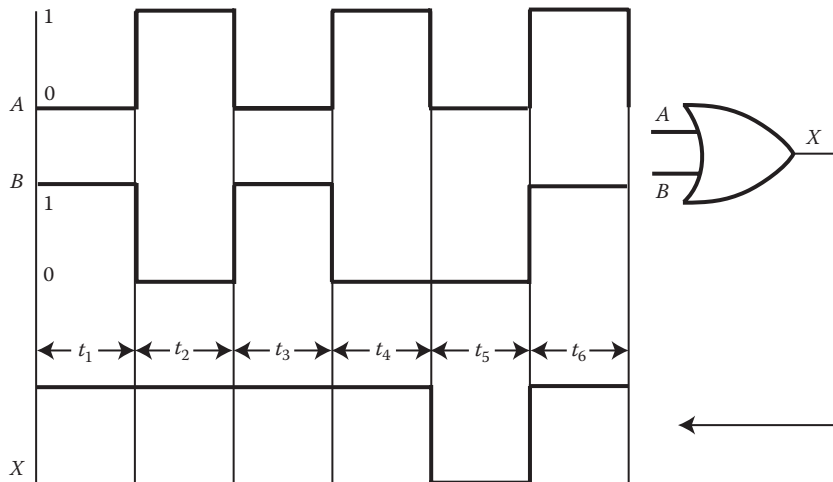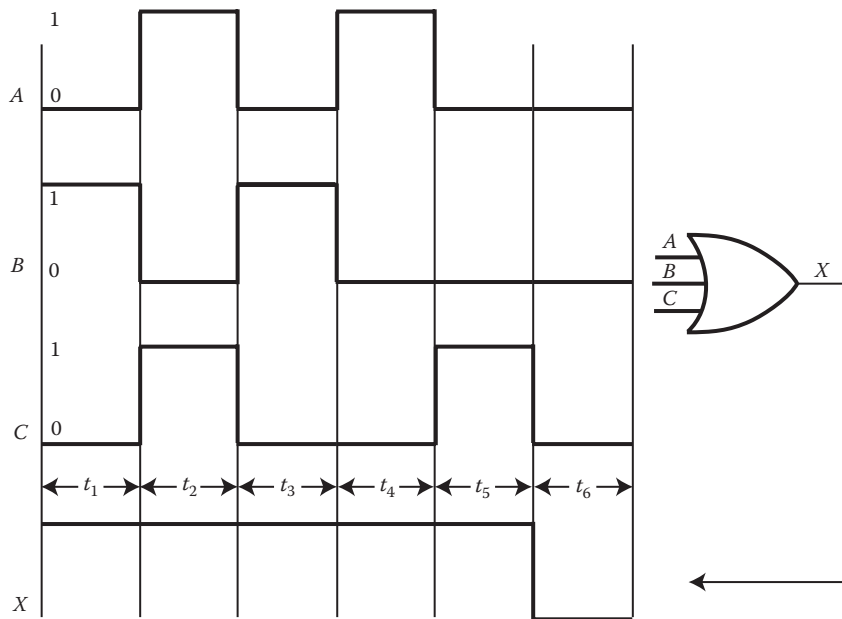Timing diagram with a 2-input OR gate.

Figure 2.20
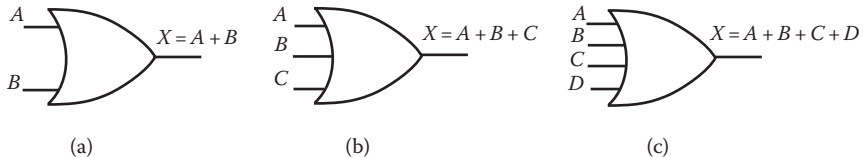Timing diagram with a 3-input OR gate.

Figure 2.21
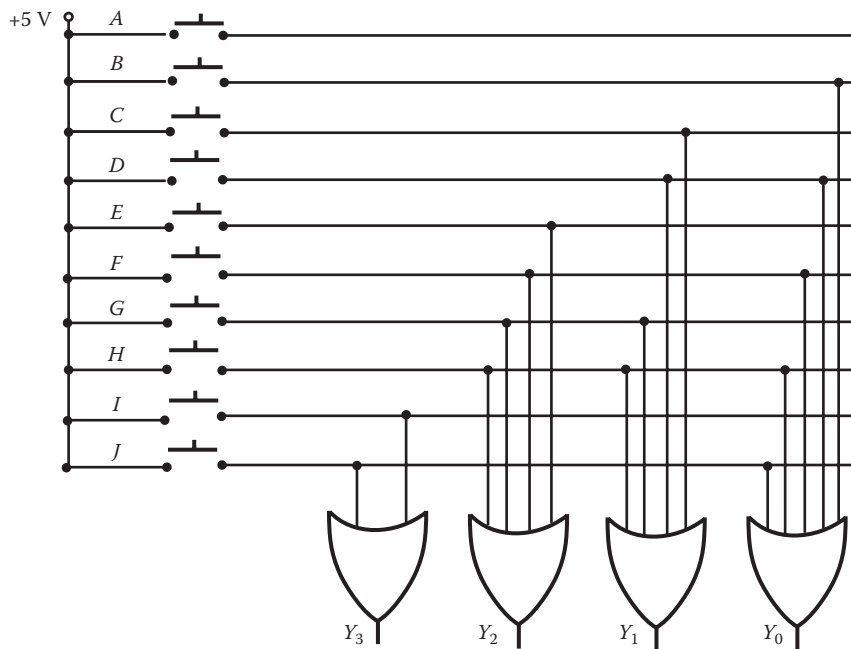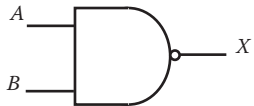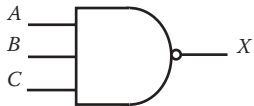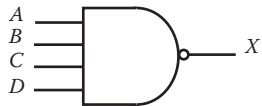Boolean expressions for OR gates with two, three, and four inputs.
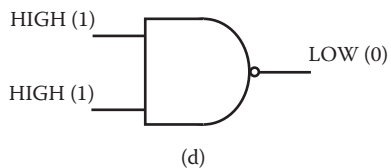
002x021.eps

Figure 2.22
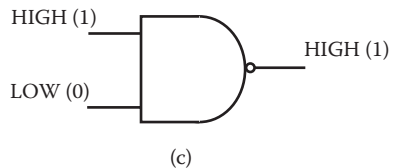Decimal-to-binary encoder.

Figure 2.23
NAND gate symbols.

Figure 2.24
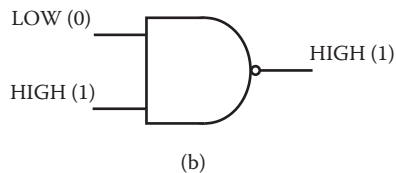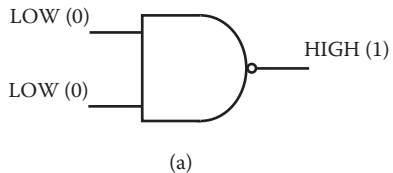Operation of a 2-input NAND gate.
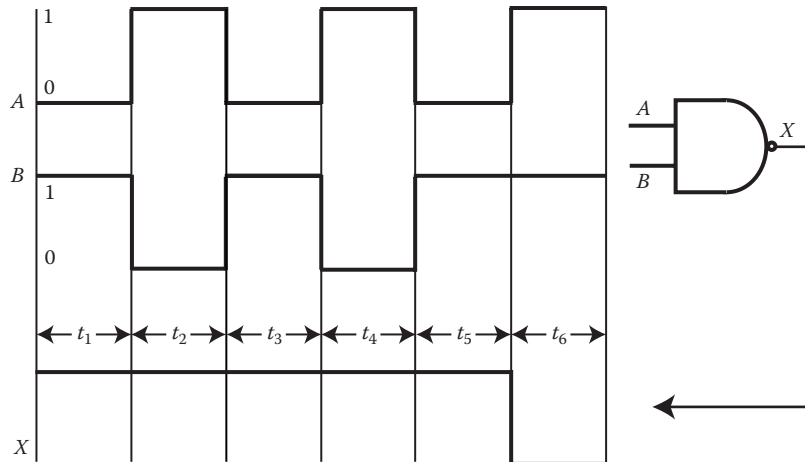
Figure 2.25
Timing diagram for a 2-input NAND gate.

NAND   Negative-OR

Figure 2.26
Standard symbols representing the two equivalent operations of a NAND gate.

002x026.eps

Figure 2.27
Timing diagram for Example 2.11.

Figure 2.28
NOR gate symbols.

Figure 2.29
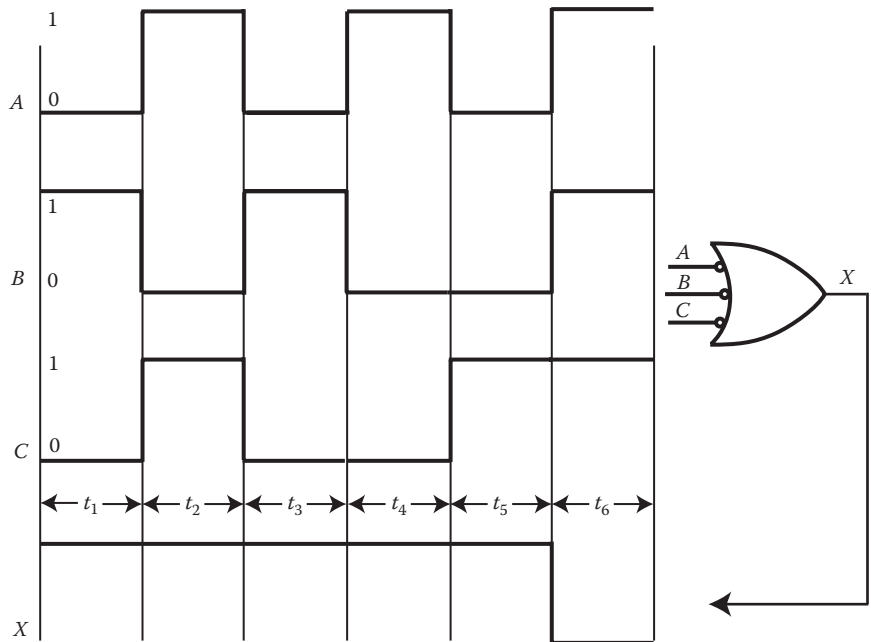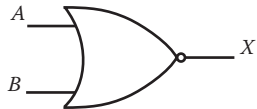Operation of a 2-input NOR gate.
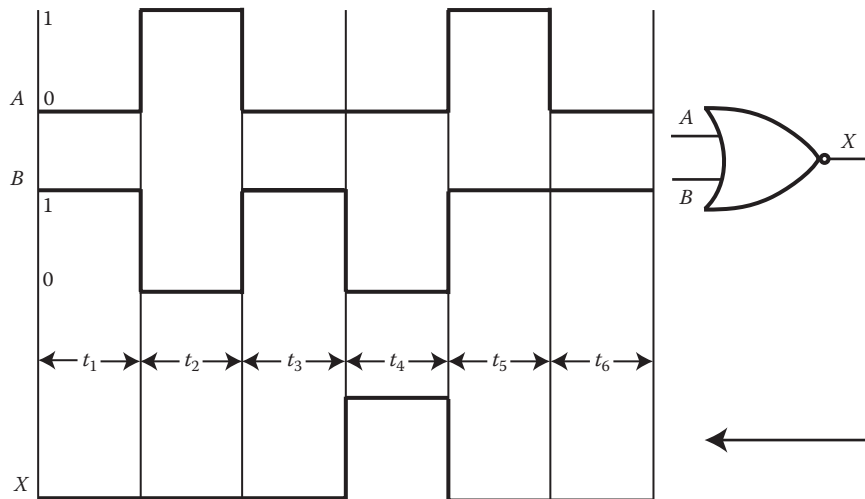
Figure 2.30
Timing diagram for a 2-input NOR gate.

NOR   Negative-AND
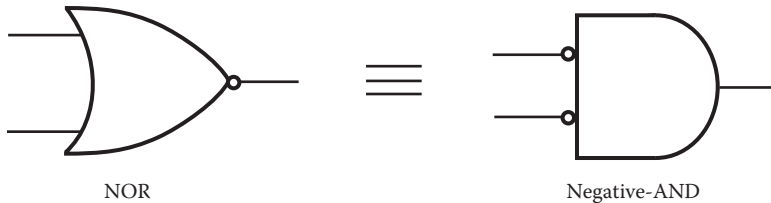
Figure 2.31
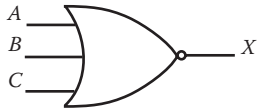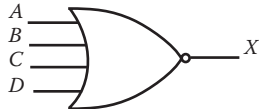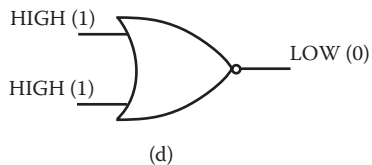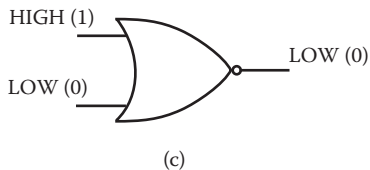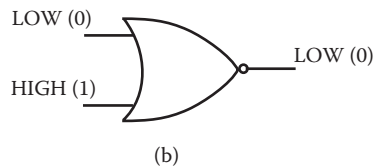Standard symbols representing the two equivalent operations of a NOT gate.

Figure 2.32
Timing diagram for Example 2.14.

Figure 2.33
XOR gate symbols.

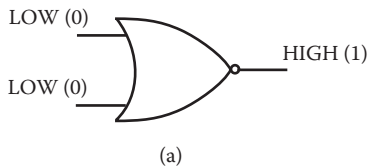LOW (0) — LOW (0) — LOW (0)

(a)

LOW (0) — HIGH (1) — HIGH (1)

(b)

HIGH (1) — LOW (0) — HIGH (1)

(c)

HIGH (1) — HIGH (1) — LOW (0)

(d)
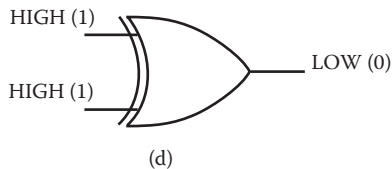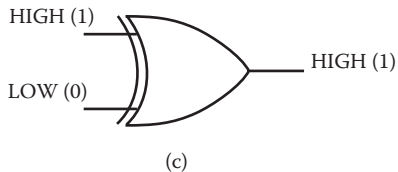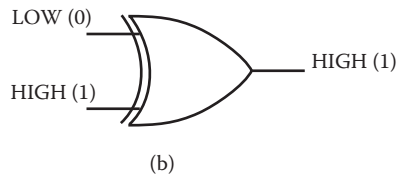
Figure 2.34
Operation of XOR gate.

Figure 2.35
(a) XOR gate, (b) a 2-input XOR gate.
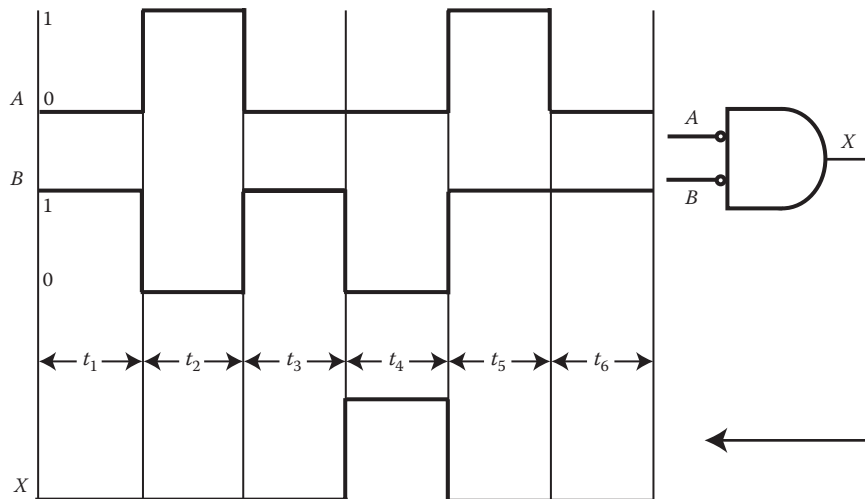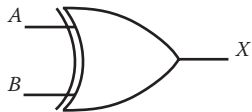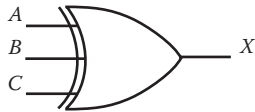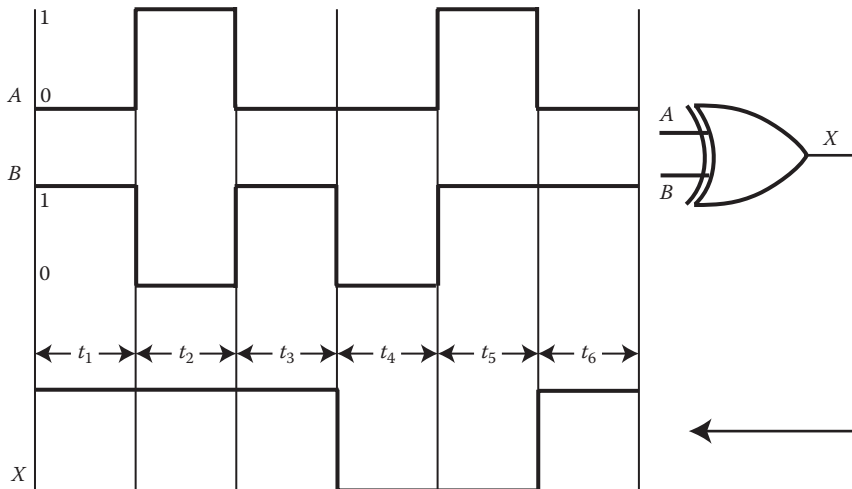
Figure 2.36
Timing diagram for XOR gate.
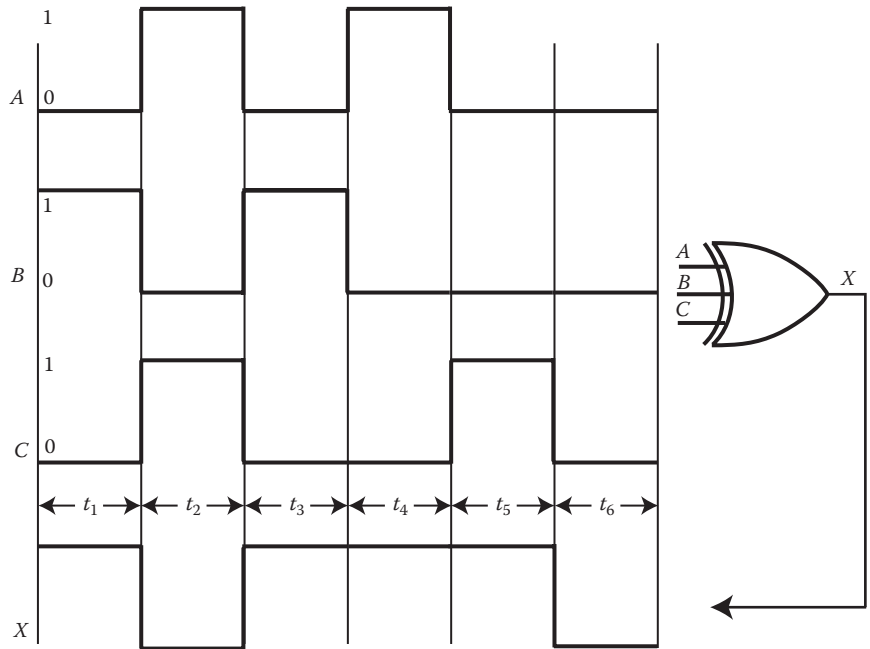
Figure 2.37
Timing diagram for XOR gate.

(a)   (b)
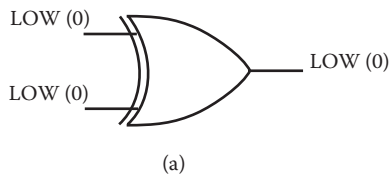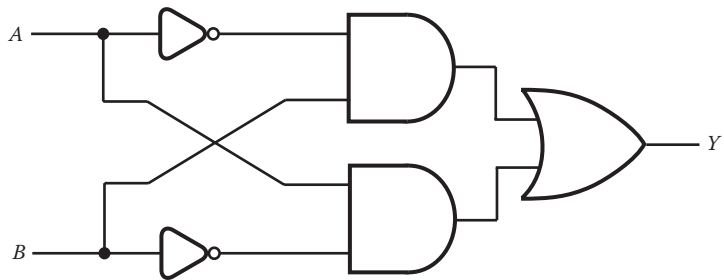
Figure 2.38
A 4-input XOR gate: (a) circuit with 2-input XOR gates, (b) equivalent logic symbol.

Figure 2.39
Odd-parity generator.

Figure 2.40
XNOR gate symbols.

002x040.eps

LOW (0)
LOW (0)
HIGH (1)

(a)

LOW (0)
HIGH (1)
LOW (0)

(b)

HIGH (1)
LOW (0)
LOW (0)

(c)

HIGH (1)
HIGH (1)
HIGH (1)
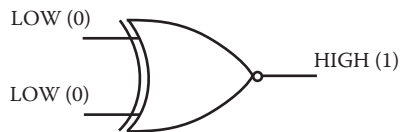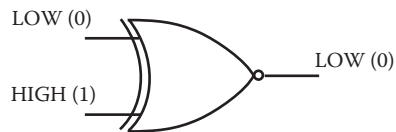
(d)

Figure 2.41
Operation of XNOR gate.
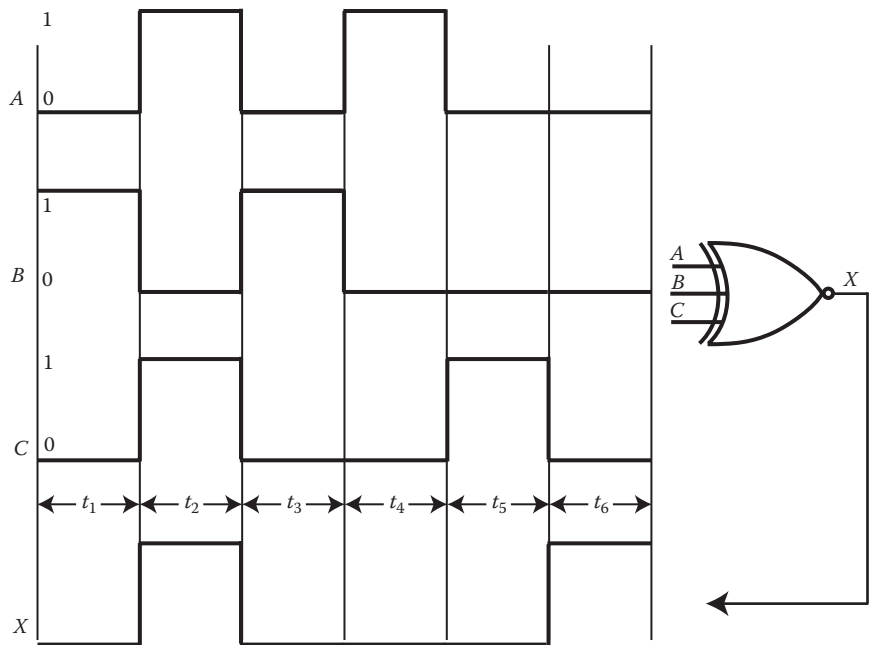
Figure 2.42
Timing diagram for XNOR gate.

AND
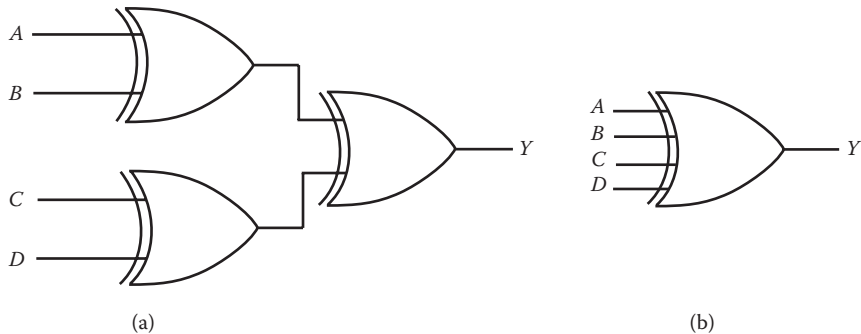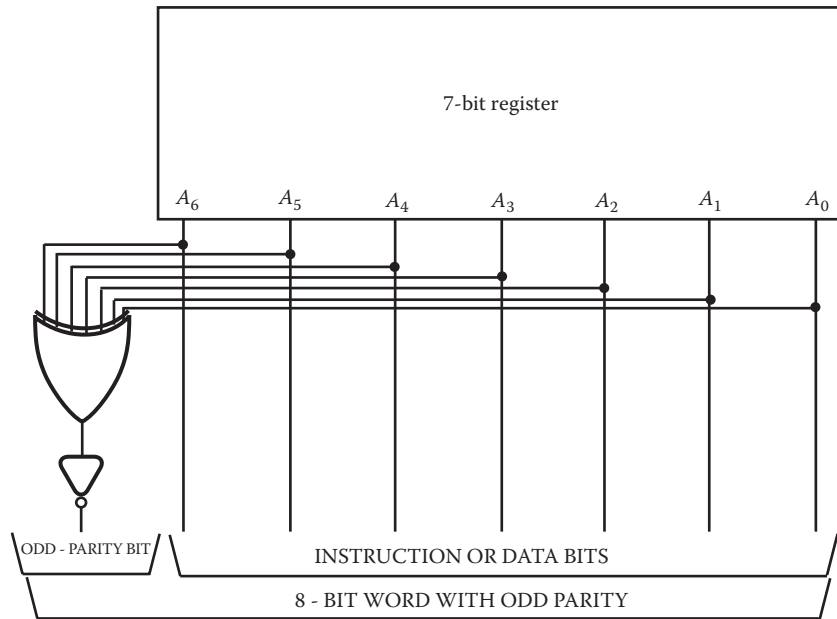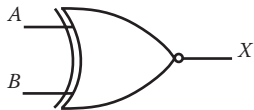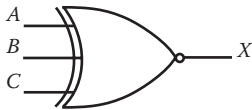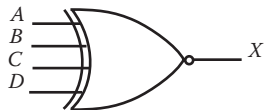
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

OR

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

NAND

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

NOT

A	X
0	1
1	0

NOR

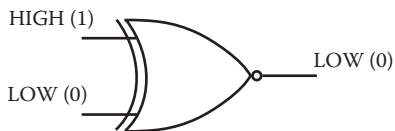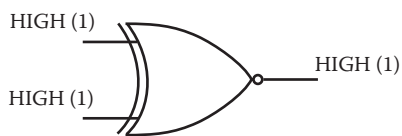| A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

XOR

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

XNOR

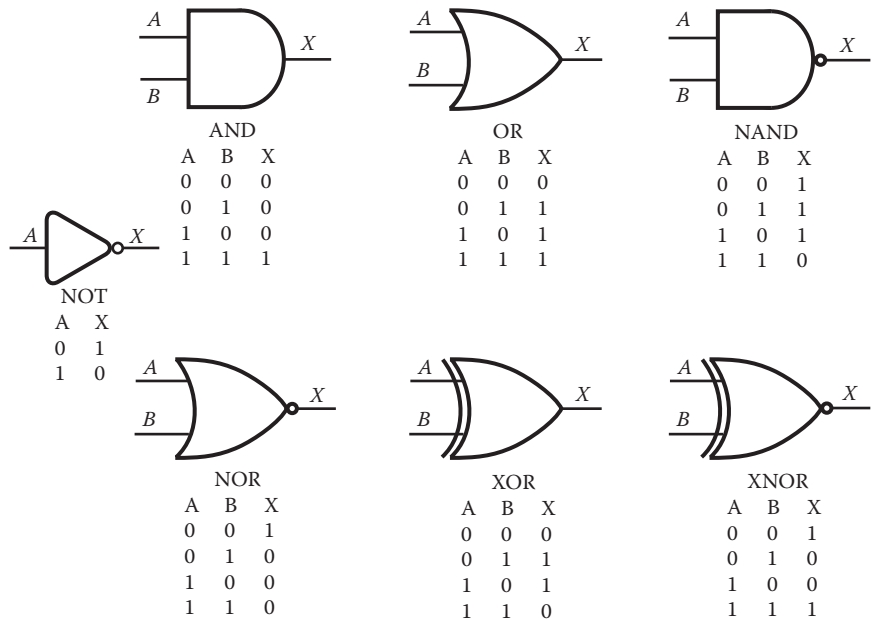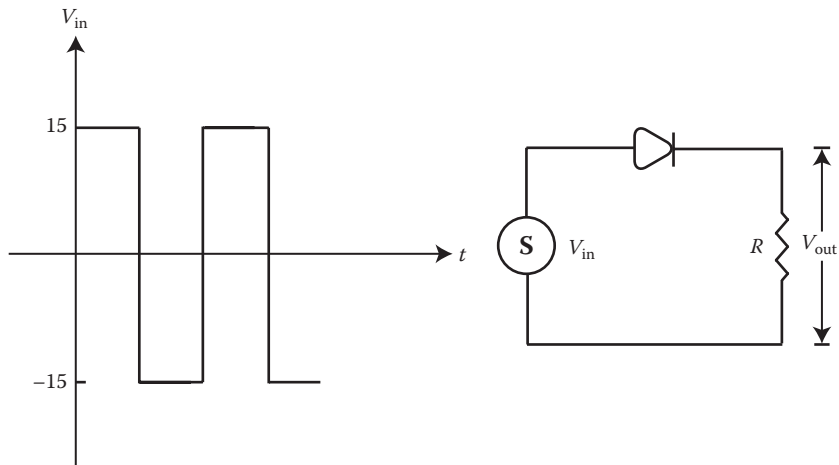| A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Figure 2.43
Summary of major gates.

Figure 2.44
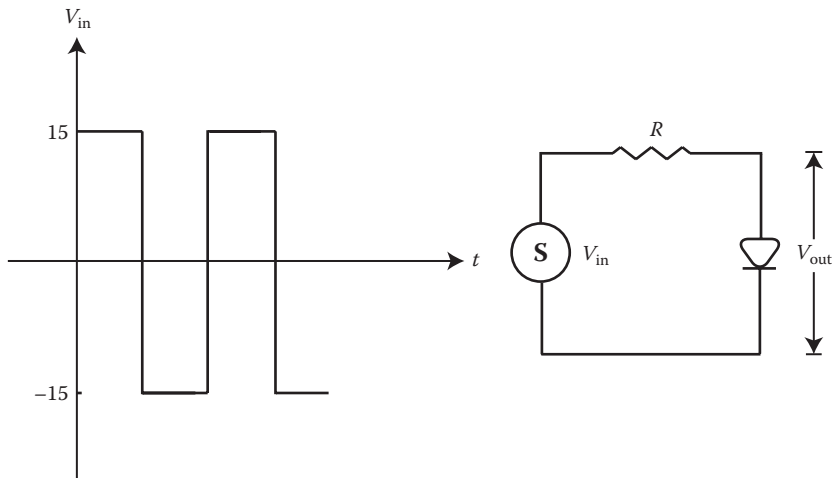Circuit diagram for Problem 2.1.

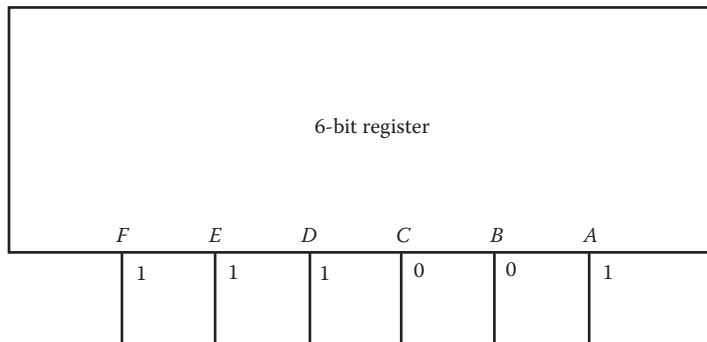002x044.eps

Figure 2.45
Circuit diagram for Problem 2.2.

Figure 2.46
Basic setup for Problem 2.3.

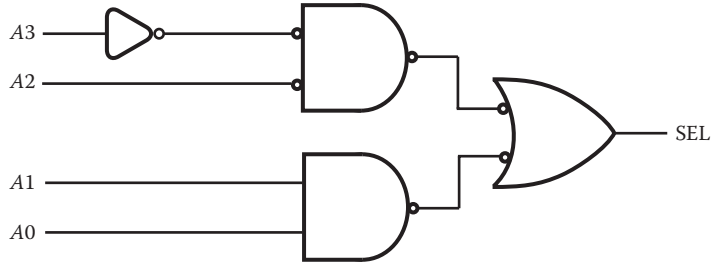Figure 2.47
Logic circuit for Problem 2.7.

Figure 2.48
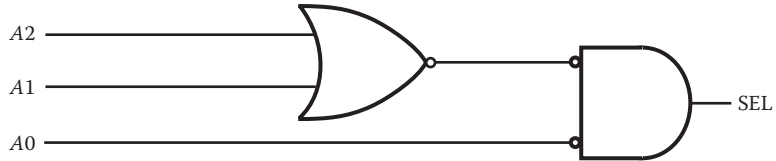Logic circuit for Problem 2.8.

BCD Digits (*W, X, Y, Z*)   Segments

(a)   (b)
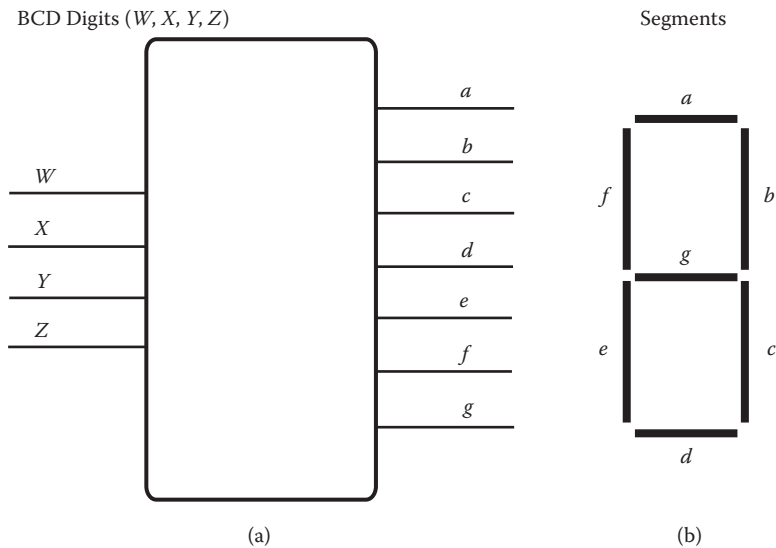
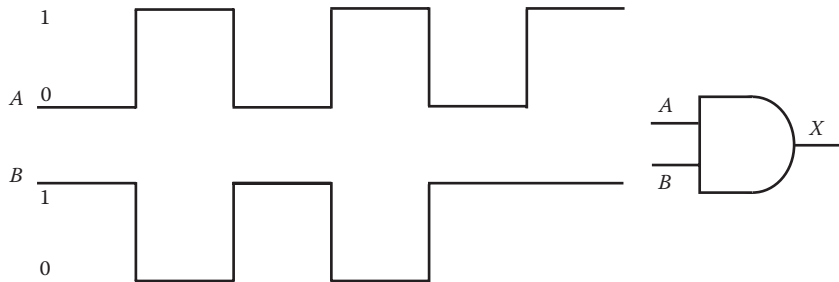Figure 2.49
Basic setup for Problem 2.9.
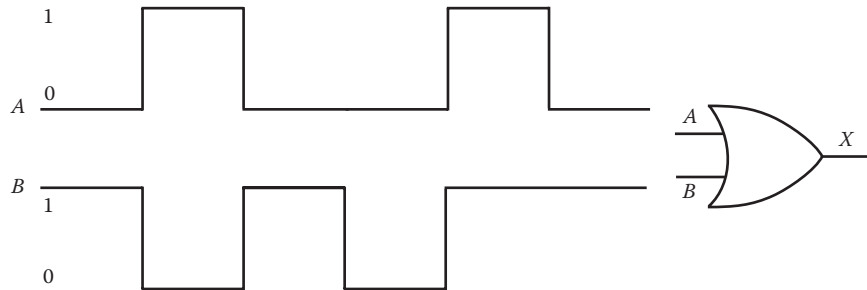
Figure 2.50
Input signals for Problem 2.11.
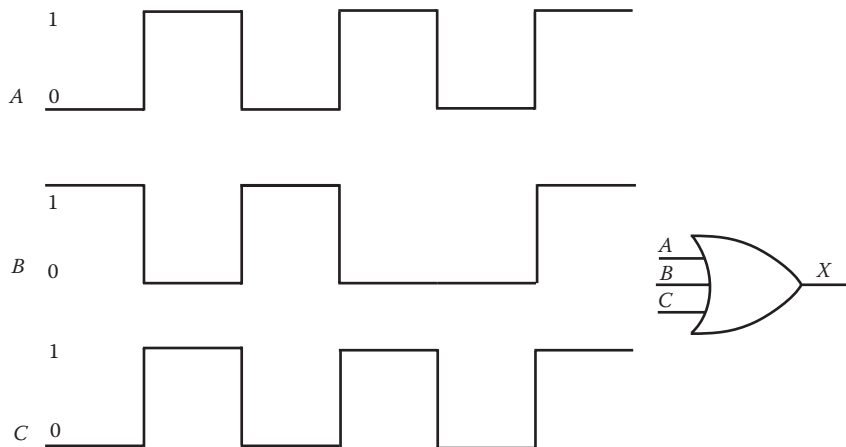
Figure 2.51
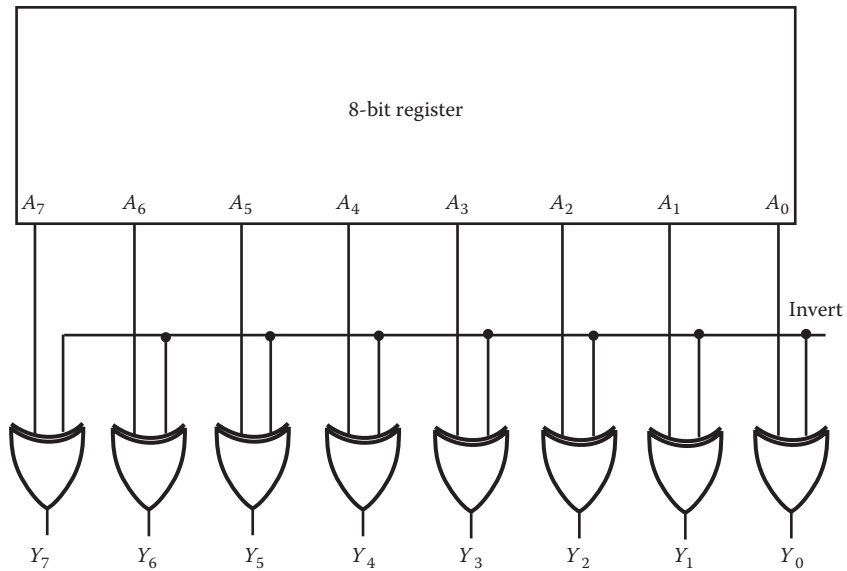Input signals for Problem 2.14.

Figure 2.52
Input signals for Problem 2.15.

Figure 2.53
A controlled inverter.