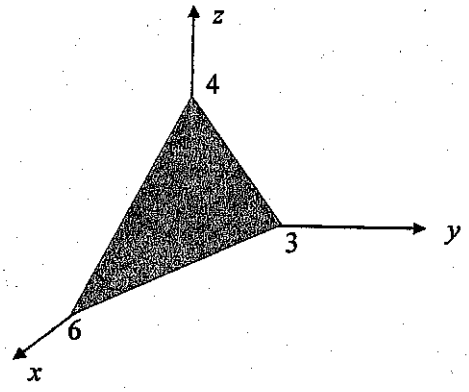
Solution to Problems

Chapter 2

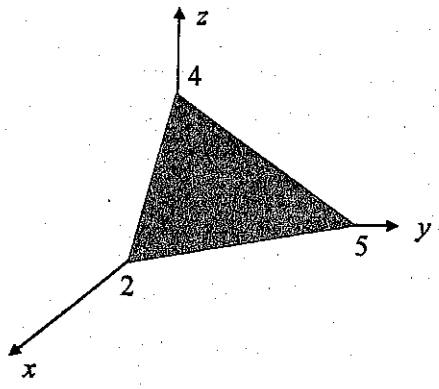
Problems for Chapter 2:

1. What is the number of the nearest-neighbor atoms for simple cubic, FCC and BCC lattice. What is the number of the second nearest neighbors for simple cubic, FCC and BCC lattice.

2. What are the Miller indices for the planes shown in figures (a) and (b)?



(a)



(b)

3. What are the Miller indices for the lines formed by the intersection of the crystal plane shown in Fig. 2b, with planes [001], [010] and [100]?

4. Find the angle α between the two nearest bonds in the diamond lattice.

5. Assume that the maximum donor concentration can be achieved when donor atoms effectively "touch" each other. The donor atoms are regarded as spheres with radii

$$a_{Bd} = a_B(\varepsilon_s/\varepsilon_0)(m_0/m_{dn})$$

where a_B=0.53 Å is the Bohr radius. Assuming that the semiconductor is GaAs, estimate the maximum doping concentration. Use $\varepsilon_s/\varepsilon_0$=12.9 and m_{dn}/m_0=0.067. **Hint:** Assume that the maximum doping level donors are as closely packed as possible, even though this is not necessarily a very realistic assumption.

6. The primitive translation vectors of the hexagonal space lattice may be taken as:

$$\mathbf{a}_1 = \sqrt{3}\frac{a}{2}\mathbf{x} + \frac{a}{2}\mathbf{y};\ \mathbf{a}_2 = -\sqrt{3}\frac{a}{2}\mathbf{x} + \frac{a}{2}\mathbf{y};\ \mathbf{a}_3 = c\mathbf{z}$$

(a) Show that the volume of the primitive cell is $\sqrt{3}/2a^2c$.

(b) Show that the primitive translation vectors of a reciprocal lattice are:

$$\mathbf{b}_1 = \frac{2\pi}{\sqrt{3}a}\mathbf{x} + \frac{2\pi}{a}\mathbf{y};\ \mathbf{b}_2 = -\frac{2\pi}{\sqrt{3}a}\mathbf{x} + \frac{2\pi}{a}\mathbf{y};\ \mathbf{b}_3 = \frac{2\pi}{c}\mathbf{z}$$

7. Show that the internal energy per unit volume of a three-dimensional Fermi gas of free particles at absolute zero is $3NE_F(0)/(5V)$; show that the corresponding result for a two-dimensional Fermi gas is $NE_F(0)/(2V)$.

8. Determine the position of the Fermi level in a *Si* sample at T=0 K, for the following doping densities:

(a) $N_A = 10^{16} cm^{-3}$, $N_D = 0$ (*p*-type sample).

(b) $N_A = 10^{16} cm^{-3}$, $N_D = 10^{15} cm^{-3}$ (compensated sample).

(c) $N_A = 10^{16} cm^{-3}$, $N_D = 10^{17} cm^{-3}$ (compensated sample).

(d) $N_A = 0$, $N_D = 10^{17} cm^{-3}$ (*n*-type sample).

Assume that both the acceptor and the donor type impurities introduce energy levels within the bandgap

9. Given an $N_A = 10^{14} cm^{-3}$ doped Si sample:

(a) Present a qualitative argument for the approximate position of the Fermi level in the material as T→0 K.

(b) Compute and plot the Fermi level as a function of T from T=300 K to T=500 K.

(c) Comment on the general position of the Fermi level as a function of T.

(d) How will the above answers be modified if the Si sample was doped with donors instead of acceptors?

10. Determine the equilibrium electron and hole concentrations inside a uniformly-doped sample of *Si* under the following conditions:

(a) Room temperature, $N_A << N_D$, $N_D = 10^{15} cm^{-3}$.

(b) Room temperature, $N_A = 10^{16} cm^{-3}$, $N_D << N_A$.

(c) Room temperature, $N_A = 9 \times 10^{15} cm^{-3}$, $N_D = 10^{16} cm^{-3}$.

(d) T=450 K, $N_A = 0$, $N_D = 10^{14} cm^{-3}$.

(e) T=650 K, $N_A = 0$, $N_D = 10^{14} cm^{-3}$.

11. Calculate the DOS function for a two-dimensional (2D) and one-dimensional (1D) system. Use the approach for the calculation of the 3D DOS function, which was described in the class. Sketch the 3D, 2D and 1D DOS functions.

12 Find the relationship between the Fermi level E_F and the electron concentration n for a 2D degenerate electron gas.

13 An effective density of states in the conduction band of silicon is equal to $2.8\times10^{19}cm^{-3}$ (at room temperature). The density of states effective mass for silicon is $1.182m_e$ at 300 K and $1.077m_e$ at 77 K, where m_e is the free electron rest mass. Consider a sample doped at $10^{16}cm^{-3}$ by shallow ionized donors. Find an expression for the number of electrons per unit energy, dn/dE, in the conduction band as a function of energy in this sample and plot it at T=77 K and T=300 K.

14 Consider a silicon sample in the thermal equilibrium at room temperature (300 K). The intrinsic carrier concentration of Si at this temperature is about $1.5\times10^{10}cm^{-3}$. Plot the concentration of electrons and holes versus acceptor doping in the range from $10^{13}cm^{-3}$ to $10^{17}cm^{-3}$ for the following shallow-donor concentrations:

(a) $10^{15}cm^{-3}$

(b) $10^{16}cm^{-3}$

15 Find the total charge of electrons injected into the p-region of a n^+p silicon diode as a function of the bias voltage V. Doping density of the p-region is N_A, intrinsic carrier concentration is n_i, and the diode temperature is T. The length of the p-region is L, and the diffusion length of electrons in the p-region is L_n. Consider three cases:

(a) Arbitrary relation between L and L_n.

(b) $L>>L_n$.

(c) $L<<L_n$.

Assume that at the contacts, $n=n_{p0}$, where n_{p0} is the equilibrium concentration of electrons.

see problem 4.1

16. Derive the expression for the space-charge region width, the maximum electric field and the depletion capacitance of a linearly graded junction.

17 Consider a pn-junction diode. The concentration of holes in the n-section of the device is described by the continuity equation

$$D_p\frac{d^2p_n}{dx^2}-\frac{p_n-p_{n0}}{\tau_p}=0\,.$$

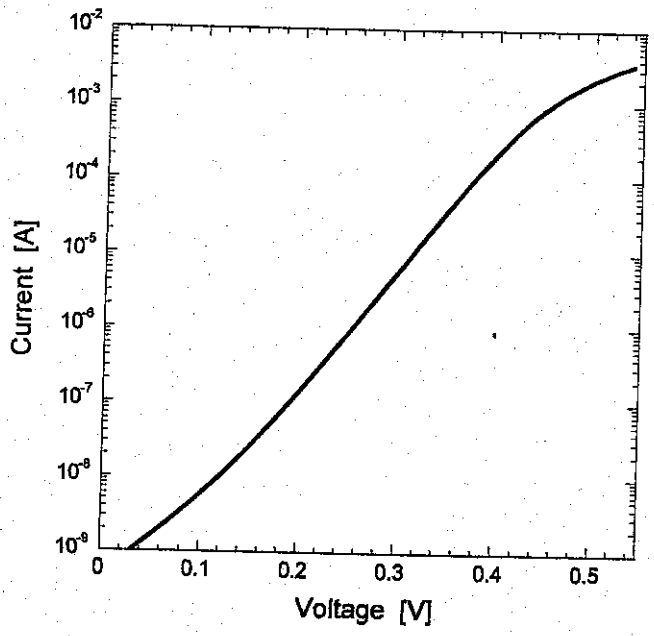
The concentration of shallow ionized donors in the n-section is equal to $10^{15}\ cm^{-3}$. The intrinsic carrier concentration is $10^{10}\ cm^{-3}$. The forward voltage applied to the diode is 0.5

V. Assuming that the length of the n-section, L, is much smaller than the diffusion length L_p, calculate and sketch the hole distribution in the n-section of the device. Also, assuming that D_p=12 cm^2/s and the lifetime τ_p=1 μs, how short does the n-section have to be to satisfy the condition that $L \ll L_p$ (use $L = L_p/10$ as a criterion)?

18 The forward IV-characteristics of a pn-diode are shown in the figure below.

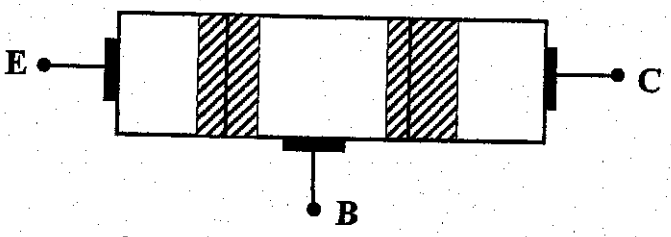
(a) Explain the origins for the deviation of the measured IV-characteristics from the ideal model predictions.

(b) Calculate the series resistance of the diode. Explain how did you arrive to your answer.

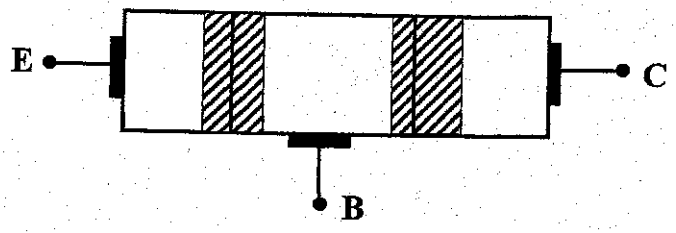


19 Show diagrammatically and with analytical expressions (the simple ones) the current components in reverse active mode and in the cut-off mode.

(a) reverse active mode:



(b) cut-off mode

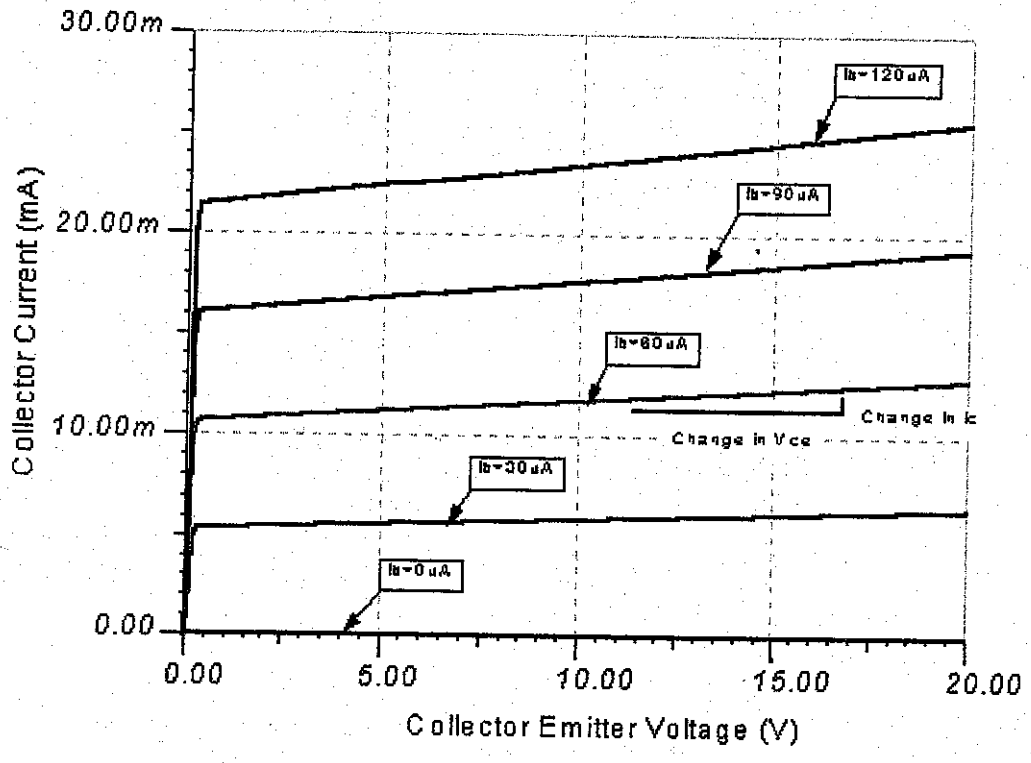


20 On the figure below are given the output characteristics of a BJT in a common-emitter configuration:

(a) What is the small signal current gain for $V_{CE} = 10$ V.

(b) What is the output conductance of this device.

(c) Estimate the Early voltage of the transistor. What is the reason for the Early effect?



21 Sketch the energy band diagram and the charge distribution in a MOS capacitor with *n*-type semiconductor for the following bias conditions:

(a) Accumulation

(b) Depletion

(c) Inversion

22. The field distribution in an ideal MOS capacitor is shown in the figure below.

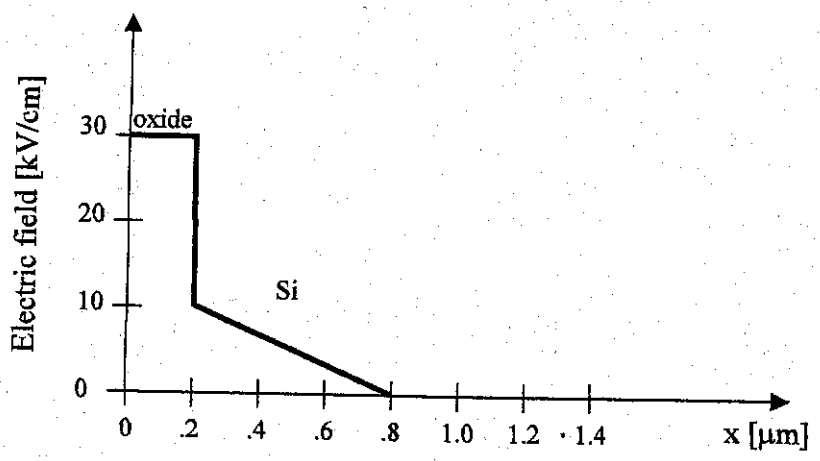
(a) Sketch the potential and the charge distribution profiles. Is the MOS capacitor biased in accumulation, depletion or inversion regime?

(b) Calculate the voltage drop in the semiconductor and in the oxide.

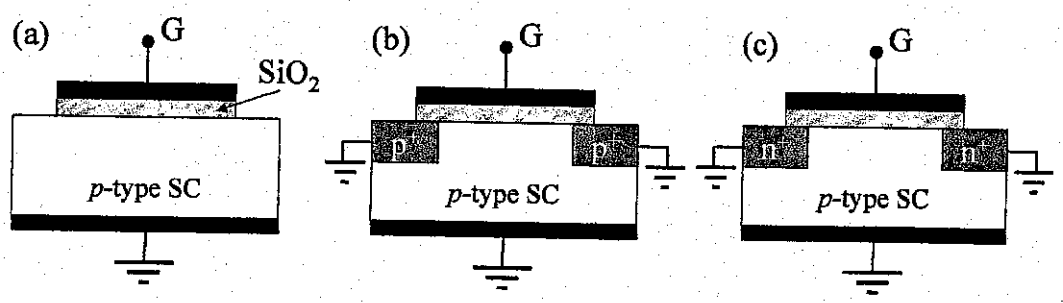
(c) What is the magnitude of the oxide capacitance C_{ox}?

(d) Calculate the threshold voltage V_{TH} for the MOS capacitor.

The dielectric permittivity of silicon is $\varepsilon_s = 1.05\times10^{-10}$ F/m, the oxide permittivity is $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m, the intrinsic carrier concentration equals to $n_i = 1.5\times10^{10}$ cm^{-3} and the temperature is T=300 K.



23. Plot the high-frequency CV-curves for the three structures shown in the figure below on the same plot. Explain how did you arrive to your answer. In your analysis assume that the gate voltage is swept very slowly.



24. Charge density 2.4×10^{-7} C/cm^2 is uniformly distributed in the oxide in a MOSFET structure. The oxide thickness is d_{ox} = 150 nm.

(a) Calculate the contribution to the threshold voltage from these charges.

(b) Calculate for the case when all charges are located at the semiconductor/oxide interface.

(c) Calculate when the charges are located 20 nm away from the semiconductor-oxide interface into the oxide layer.

In your calculations, for the dielectric permittivity of the oxide use $\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m.

25 Charge density of 2.4×10^{-7} Coulombs/cm^2 is uniformly distributed in the oxide in a MOSFET structure. The oxide thickness is d_{ox}=150 nm.

same problem as 24

(a) Calculate the contribution to the threshold voltage from these oxide charges.

(b) Calculate for the case when all the charges are located at the silicon-silicon dioxide interface.

(c) Calculate for the linear charge distribution within the oxide (zero charge density at the *Si-SiO₂* interface, maximum charge density at the metal-*SiO₂* interface).

26 Consider nearly two identical silicon MOSFETs. The only difference between the two devices is that the oxide layer in one of them is perfectly clean, and the other one is contaminated with sodium ions that produce a positive charge density. The concentration of sodium ions equals to $2 \times 10^{16} cm^{-3}$, and the thickness of the oxide layer is 0.1 μm. The permittivity of SiO_2 is $3.45 \times 10^{-11} F/m$.

(a) What is the difference (including sign) in the device threshold voltages if these devices are *n*-channel devices?

(b) What is the difference (including sign) in the device threshold voltages if these devices are *p*-channel devices?

(c) Assume that the threshold voltage of the *n*-channel clean device is 1 V and that the threshold voltage of the *p*-channel clean device is -1 V. Sketch the qualitative dependencies of the drain-to-source saturation current on the gate voltage for all four devices (clean and contaminated *n*-channel and clean and contaminated *p*-channel devices). Label the thresholds and shifted thresholds on the gate-voltage axis.

27 Derive the expressions for the extrinsic transconductance and the extrinsic drain conductance of a transistor with finite source and drain series resistances in terms of those of an ideal transistor with zero series resistances.

28 Calculate the dependence of the drain current I_D upon the drain voltage V_{DS} for V_{GS} = 5 V, for a silicon MOSFET with the following values of the source (R_S) and drain

resistance (R_D): $R_S = R_D = 0\ \Omega$, and $R_S = R_D = 100\ \Omega$. The device parameters are as follows:

gate length: $L = 4\ \mu m$

gate width: $W = 100\ \mu m$

electron mobility in the channel: $\mu_n = 1000\ cm^2/V\text{-}s$

dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}\ F/m$

dielectric permittivity of silicon: $\varepsilon_{sc} = 1.05\times10^{-10}\ F/m$

flat-band voltage: $V_{FB} = 0\ V$

substrate bias: $V_{sub} = 0\ V$

temperature: $T = 300\ K$

substrate doping: $N_A = 10^{15}\ cm^{-3}$

gate oxide thickness: $d_{ox} = 20\ nm$

intrinsic carrier concentration: $n_i = 1.5\times10^{10}\ cm^{-3}$

In your calculations use:

(a) square-law theory

(b) bulk-charge theory

Repeat the problem for $N_A=10^{16}\ cm^{-3}$ and $N_A=10^{17}\ cm^{-3}$. Discuss the validity of the square-law theory versus substrate doping and the influence of the series resistance on the drain current characteristics of these devices.

29 Derive an expression for the drain saturation current of an *n*-channel MOSFET using square-law theory and neglecting velocity saturation effects, i.e. assuming the constant mobility model, but taking into account the source series resistance R_S. Use the following MOSFET parameters:

gate oxide thickness: $d_{ox} = 17.5\ nm$

device gate width: $W = 100\ \mu m$

gate length: $L = 4\ \mu m$

threshold voltage: $V_T = -1\ V$

electron mobility in the channel: $\mu_n = 800\ cm^2/V\text{-}s$

dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}\ F/m$

gate voltage: $V_{GS} = 5\ V$

substrate bias: $V_{sub} = 0\ V$

Plot I_{Dsat} versus R_S for $2\Omega < R_S \leq 20\ \Omega$.

30 Calculate and plot the subthreshold current for a long-channel Si MOSFET as a function of the gate voltage V_{GS} that varies in the range between V_T - 1 (V) and V_T. For the drain voltage assume V_{DS} = 0.01 V, 0.1 V, and 10 V. Use the following parameters:

threshold voltage: $V_T = 1$ V

substrate doping: $N_A = 10^{15}$ cm^{-3}

electron mobility in the channel: : $\mu_n = 800$ cm^2/V-s

device gate width: $W = 100$ μm

gate length: $L = 20$ μm

gate oxide thickness: $d_{ox} = 50$ nm

energy band gap: $E_G = 1.12$ eV

effective density of states in the conduction band: $N_C = 3.22\times10^{19}$ cm^{-3}

effective density of states in the valence band: $N_V = 1.83\times10^{19}$ cm^{-3}

dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m

dielectric permittivity of silicon: $\varepsilon_{sc} = 1.05\times10^{-10}$ F/m

temperature: $T = 300$ K

31 Consider the following idealized ion implantation profile near the semiconductor-insulator interface in a Si MOSFET ($x = 0$ corresponds to the semiconductor insulator interface). Calculate the threshold voltage shift as a function of N_i, for 10^{14} cm^{-3} ≤ N_i ≤ 10^{17} cm^{-3} for $d_{imp} = 0.08$ μm. Assume:

semiconductor background doping $N_A = 10^{15}$ cm^{-3}

gate oxide thickness: $d_{ox} = 50$ nm

energy band gap: $E_G = 1.12$ eV

effective density of states in the conduction band: $N_C = 3.22\times10^{19}$ cm^{-3}

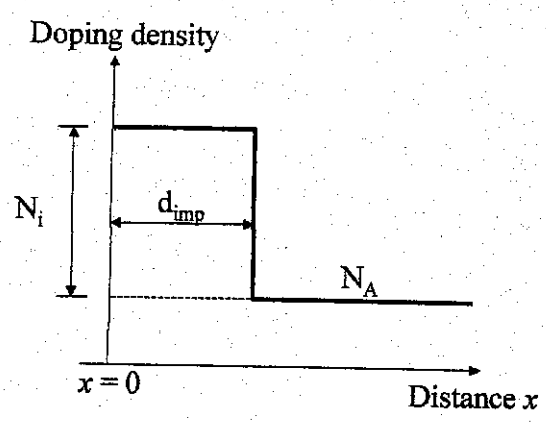
effective density of states in the valence band: $N_V = 1.83\times10^{19}$ cm^{-3}

dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m

dielectric permittivity of silicon: $\varepsilon_{sc} = 1.05\times10^{-10}$ F/m

temperature: $T = 300$ K

Assume shallow ionized acceptors. Define the threshold voltage as the gate voltage for which the electron concentration at the surface $n(0)$ is equal to $N_A + N_i$.



32 The current-voltage characteristics of a long-channel MOSFET are described with:

$$I_D = \begin{cases} \dfrac{Z\mu_{eff}C_{ox}}{L}\left[(V_G - V_T)V_D - \dfrac{1}{2}V_D^2\right], & V_D < V_G - V_T \\ \dfrac{Z\mu_{eff}C_{ox}}{2L}(V_G - V_T)^2, & V_D > V_G - V_T \end{cases}$$

where μ_{eff} is the effective electron mobility in the channel, L is the effective channel length, Z is the channel (gate) width, C_{ox} is the gate capacitance, I_D is the drain current, V_D is the drain voltage (with the source as reference), V_G is the gate voltage, and V_T is the threshold voltage. When the drain and gate are connected, consider the following two cases:

(a) $V_T > 0$, and

(b) $V_T < 0$.

Find and plot I_D in terms of V_D in each of these two cases.

34 A GaAs MESFET is fabricated using an epitaxial layer doped to $N_D = 10^{17}$ cm^{-3} that is 0.2 μm thick. The Schottky barrier metallization has a barrier height of 0.75 eV.

(a) Evaluate the built-in voltage V_{bi}.

(b) Evaluate the pinch-off voltage V_{po}.

(c) Evaluate the threshold voltage V_T.

(d) Is the resulting transistor a depletion or enhancement mode device?

(e) What is the depletion layer thickness with zero gate voltage?

35 Write a program to evaluate the drain current as a function of V_D for a specified gate voltage. Use the transistor parameters of problem 34. The program should be valid for all channel lengths; assume that $\mu_n = 5000$ cm^2/V-s and $v_s = 1.3\times10^7$ cm/s.

a. Plot $I_D(V_D)$ with $V_G = 0$ for a transistor with L= 10 μm and Z = 100 μm.

b. Repeat (a) for L = 0.2 μm and Z = 100 μm.

c. Compare V_{Dsat} in (b) with the value $V_{Dsat} = E_sL$ which is the extreme velocity saturation limit. Does this limit apply to a transistor with L = 0.2 μm?